

Exhibit 8

Western Digital Accused Products

The following list of Accused Products is exemplary, non-exhaustive, and non-limiting. Greenthread asserts claims against all product variations and part numbers of the Accused Products.

| | Solid State Drives (SSDs) |
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| 1. | WD_BLACK SN850X NVMe™ SSD |
| 2. | SanDisk Extreme PRO Portable SSD V2 |
| 3. | My Passport™ SSD |
| 4. | PRO-BLADE TRANSPORT |
| 5. | WD_BLACK SN850 NVMe™ SSD for PS5™ Consoles |
| 6. | SanDisk Ultra 3D SSD |
| 7. | SanDisk Extreme Portable SSD V2 |
| 8. | WD Blue SA510 SATA SSD 2.5"/7mm Cased |
| 9. | PRO-BLADE SSD Mag |
| 10. | WD_BLACK P40 Game Drive SSD |
| 11. | WD Green SN350 NVMe™ SSD |
| 12. | G-DRIVE SSD |
| 13. | WD_BLACK SN770 NVMe™ SSD |
| 14. | SanDisk® Portable SSD |
| 15. | WD Red SN700 NVMe SSD |
| 16. | WD Blue SA510 SATA SSD M.2 2280 |
| 17. | WD_BLACK™ D30 Game Drive SSD for Xbox™ |
| 18. | SanDisk SSD Plus |
| 19. | WD_BLACK SN750 NVMe™ SSD |
| 20. | WD Green™ SATA SSD 2.5"/7mm Cased |
| 21. | WD Red™ SA500 NAS SATA SSD M.2 2280 |
| 22. | WD Elements™ SE SSD |
| 23. | WD Blue™ SATA SSD 2.5"/7mm cased |
| 24. | WD_BLACK P50 Game Drive SSD |
| 25. | WD Red™ SA500 NAS SATA SSD 2.5"/7mm Cased |
| 26. | WD_BLACK D50 Game Dock NVMe™ SSD |

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| 27. | WD Blue™ SATA SSD M.2 2280 |
| 28. | WD_BLACK D30 Game Drive SSD |
| 29. | WD Green™ SATA SSD M.2 2280 |
| 30. | OpenFlex Data24 NVMe-oF Storage Platform |
| 31. | Ultrastar Edge Transportable Edge Server |
| 32. | Ultrastar Edge-MR Ruggedized Edge Server |
| 33. | WD Gold™ Enterprise Class NVMe™ SSD |
| 34. | Ultrastar DC SN640 |
| 35. | Ultrastar DC SA210 |
| 36. | Ultrastar DC SN840 |
| 37. | Ultrastar DC ZN540 |
| 38. | Western Digital PC SN810 NVMe SSD |
| 39. | Western Digital CL SN520 NVMe SSD |
| 40. | WD Blue SN570 NVMe™ SSD |
| 41. | G-DRIVE™ PRO STUDIO SSD |
| 42. | PC SN540 NVMe SSD |
| 43. | PRO-G40 SSD |
| 44. | RapidFlex NVMe™-oF Controllers - A2000 |
| 45. | RapidFlex NVMe™-oF Controllers - C2000 |
| 46. | Western Digital PC SN740 NVMe™ SSD |
| 47. | Western Digital PC SA510 SATA SSD |
| 48. | Ultrastar DC SN650 |
| 49. | PRO-BLADE STATION |
| 50. | SanDisk Extreme PRO M.2 NVMe 3D SSD |
| 51. | SanDisk Extreme Pro® Portable SSD |
| 52. | WD_BLACK - The Game Awards Limited Edition |
| 53. | WD_BLACK D50 Game Dock |
| 54. | WD_BLACK AN1500 NVMe SSD Add-in-Card |
| 55. | WD_BLACK SN850 NVMe™ SSD |
| 56. | WD® Gaming Drive Accelerated for Xbox One™ |
| 57. | WD_BLACK™ Call of Duty®: Black Ops Cold War Special Edition P50 Game Drive NVMe™ SSD |

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| 58. | WD_BLACK™ Call of Duty®: Black Ops Cold War Special Edition SN850 NVMe™ SSD |
| 59. | easystore SSD |
| 60. | G-DRIVE ArmorLock SSD |
| 61. | G-DRIVE PRO SSD |
| 62. | G-RAID SHUTTLE SSD |
| 63. | WD_BLACK SN750 SE NVMe™ SSD Battlefield™ 2042 PC Game Code Bundle |
| 64. | RapidFlex NVMe™-oF Controllers - A1000 |
| 65. | RapidFlex NVMe™-oF Controllers - C1000 |
| 66. | PC SA530 3D NAND SATA SSD |
| 67. | PC SN530 NVMe SSD |
| 68. | PC SN730 NVMe SSD |
| 69. | easystore SSD Portable Storage |
| 70. | Industrial NVMe SSD |
| | USB Flash Drives |
| 71. | SanDisk Ultra® Dual Drive Luxe USB Type-C™ Flash Drive |
| 72. | SanDisk Ultra Dual Drive Go USB Type-C, Rainbow Pride Limited Edition |
| 73. | SanDisk Ultra Eco™ USB 3.2 Flash Drive |
| 74. | Ultra Dual Drive USB 3.0 |
| 75. | Ultra Dual Drive m3.0 |
| 76. | SanDisk Ultra Luxe™ USB 3.1 Flash Drive |
| 77. | SanDisk Ultra Flair USB 3.0 Flash Drive |
| 78. | SanDisk Ultra USB 3.0 Flash Drive |
| 79. | Cruzer Glide 3.0 USB Flash Drive |
| 80. | Cruzer Force USB Flash Drive |
| 81. | Cruzer Glide USB Flash Drive |
| 82. | Cruzer Blade USB Flash Drive |
| 83. | Cruzer Fit USB Flash Drive |
| 84. | SanDisk Ultra Fit USB 3.2 Flash Drive |
| 85. | Ultra Dual Drive Go USB Type-C™ |

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|---------------------|--|
| 86. | SANDISK® CRUZER SPARK™ USB 2.0 Flash Drive |
| 87. | SanDisk Ultra® USB Type-C™ Flash Drive |
| 88. | SanDisk® Ultra Shift™ USB 3.0 Flash Drive |
| 89. | iXpand™ Flash Drive Flip |
| 90. | SanDisk® iXpand® Flash Drive Luxe |
| 91. | SanDisk Extreme PRO® USB 3.2 Solid State Flash Drive |
| 92. | easystore USB |
| 93. | iXpand Flash Drive Go |
| 94. | Ultra Dual Drive USB Type-C |
| 95. | SanDisk Extreme Go USB 3.1 Flash Drive |
| 96. | SanDisk Extreme Go USB Drive |
| Memory Cards | |
| 97. | SanDisk Extreme® microSDXC™ UHS-I CARD |
| 98. | SanDisk Extreme Pro CFexpress® Card Type B |
| 99. | Nintendo®-Licensed Memory Cards For Nintendo Switch™ |
| 100. | SanDisk MAX ENDURANCE microSD™ Card |
| 101. | SanDisk microSDXC™ card for Nintendo Switch™, Fortnite® Edition |
| 102. | SanDisk Extreme SD UHS-I Card |
| 103. | SanDisk Extreme PRO SDXC™ UHS-II Card |
| 104. | SanDisk Professional PRO-READER SD and microSD™ |
| 105. | SanDisk Extreme PRO microSDXC™ UHS-I CARD |
| 106. | SanDisk Extreme PRO® SDHC™ and SDXC™ UHS-II cards |
| 107. | PRO-CINEMA CFexpress® VPG400 Type B |
| 108. | SanDisk Extreme SD UHS-I Card (Up to 150 MBPs) |
| 109. | SanDisk Extreme PRO® SDHC™ And SDXC™ UHS-I Card (Up to 170 MBPs) |
| 110. | SanDisk Extreme microSDXC™ UHS-I CARD (Up to 160 MBPs) |
| 111. | SanDisk Extreme PRO microSDXC™ UHS-I CARD (Up to 170 MBPs) |
| 112. | SanDisk Extreme microSD™ Card for Mobile Gaming (Up to 160 MBPs) |
| 113. | SanDisk Ultra® microSD™ Card for Chromebook |
| 114. | SanDisk Ultra microSD with SD Adapter |
| 115. | SanDisk Ultra® SDHC™ UHS-I card and SDXC™ UHS-I card |

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| 116. | SDHC/SDXC Memory Card |
| 117. | SanDisk High Endurance microSD™ Card |
| 118. | WD Purple SC QD101 Ultra Endurance microSD Card |
| 119. | SanDisk Extreme microSD™ Card for Mobile Gaming |
| 120. | SanDisk Extreme Pro CFexpress® Card Type B |
| 121. | SanDisk Ultra® SDHC™ UHS-I card and SDXC™ UHS-I card (Up to 120MBPs) |
| 122. | SanDisk Ultra microSD with SD Adapter (Up to 120MBPs) |
| 123. | Extreme CompactFlash Memory Card |
| 124. | Extreme Pro CompactFlash Memory Card |
| 125. | SanDisk Extreme PRO CFast 2.0 Memory Card |
| 126. | SanDisk Extreme PRO SDHC™ And SDXC™ UHS-I Card |
| 127. | SanDisk Ultra® microSD™ Card for Chromebook (Up to 120MBPs) |
| 128. | SanDisk Extreme PRO® SDHC™ And SDXC™ UHS-I Card |
| 129. | SanDisk Ultra microSD UHS-I Card |
| 130. | Ultra SDHC/SDXC Memory Card |
| 131. | SanDisk® microSDXC™ card for Nintendo Switch™, Apex Legends |
| 132. | SanDisk Extreme PRO® UHS-II Card |
| 133. | Commercial Edge SD Card |
| 134. | Commercial Edge microSD Card |
| 135. | Industrial microSD Card |
| 136. | Industrial SD Card |
| 137. | Automotive SD Card |
| 138. | Connected Home Edge+ SD Card |
| 139. | Connected Home Edge+ microSD Card |
| | Data Center Storage |
| 140. | WD Gold™ Enterprise Class NVMe™ SSD |
| 141. | Embedded Flash |
| 142. | Connected Home e.MMC |
| 143. | Automotive e.MMC |
| 144. | Commercial UFS |
| 145. | Automotive UFS |

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| 146. | Commercial e.MMC |
| 147. | Industrial UFS |
| 148. | Industrial e.MMC |
| | Network Attached Storage |
| 149. | WD Red SN700 NVMe SSD |
| 150. | WD Red™ SA500 NAS SATA SSD 2.5"/7mm Cased |

Exhibit A-1 to Greenthread's Complaint









| U.S. Patent No. 10,510,842 | Accused Products |
|---|--|
| <p>[Claim 1, Preamble] A semiconductor device, comprising:</p> | <p>To the extent the preamble is a limitation, the Western Digital Accused Products include a semiconductor device. For example, as shown below, the Defendants sell various examples of flash memory devices (e.g., microSD/SD cards and solid-state drives (SSDs), both of which contain flash memory).</p> <p>Below are examples of SanDisk SDHC (SD High Capacity) flash memory cards:</p> <div data-bbox="905 375 1604 1357"> <div data-bbox="905 375 1241 1357"> <p>Is this relevant?   </p> <p><input type="checkbox"/> Compare</p>  <p>SanDisk - Flash memory card - 32 GB - Class 4 - SDHC</p> <p>★★★★☆ 4.2 (28)</p> <p>\$10.99</p> <p>Get it as soon as Monday, May 2</p> <p>View Delivery Dates for 20170</p> <p>Manufacturer Part SDSDB-032G-A46 Dell Part A7610910</p> <p>View Details</p> </div> <div data-bbox="1268 375 1604 1357"> <p>Is this relevant?   </p> <p><input type="checkbox"/> Compare</p>  <p>SanDisk - Flash memory card - 16 GB - Class 4 - SDHC</p> <p>★★★★☆ 4.5 (15)</p> <p>\$10.99</p> <p>Get it as soon as Monday, May 2</p> <p>View Delivery Dates for 20170</p> <p>Manufacturer Part SDSDB-016G-A46 Dell Part A7610909</p> <p>View Details</p> </div> </div> <p>See https://www.dell.com/en-us/search/flash%20memory</p> <p>Below is an example of a SanDisk SSD:</p> |

Exhibit A-1 to Greenthread's Complaint




| U.S. Patent No. 10,510,842 | Accused Products |
|----------------------------|---|
| | <div data-bbox="667 354 787 625">  </div> <div data-bbox="1123 199 1843 280"> <h3>SanDisk Extreme Portable - Solid state drive - 500 GB - external (portable) - USB 3.1 Gen 2</h3> </div> <div data-bbox="1123 318 1843 402"> <p>Your life's an adventure. The SanDisk Extreme Portable SSD fits your mobile lifestyle and accelerates every move. Nearly 2x as fast as our previous generation!</p> </div> <div data-bbox="1123 418 1444 487"> <p>Estimated Value \$139.99 \$119.99 You Save \$20.00 (14%)</p> </div> <div data-bbox="1123 516 1381 565"> <p>Get it as soon as Friday, Apr 29 View Delivery Dates for 95050</p> </div> <div data-bbox="1123 597 1612 662"> <p> Financing As low as \$20/mo.* Apply for Credit  Up to \$3 back in rewards</p> </div> <div data-bbox="1123 695 1648 747"> <div data-bbox="1123 695 1245 747">1 ▾</div> <div data-bbox="1312 695 1648 747">Add to Cart</div> </div> <div data-bbox="1123 771 1806 792"> <p>Manufacturer Part SDSSDE61-500G-G25 Dell Part AB609642 Order Code Ab609642 SanDisk</p> </div> <div data-bbox="1123 824 1255 849"> <p><input type="checkbox"/> Compare</p> </div> <div data-bbox="1060 914 1255 954"> <h2>Tech Specs</h2> </div> <div data-bbox="1060 1036 1171 1071"> <h3>General</h3> </div> <div data-bbox="1060 1112 1417 1185"> <p>Device Type Solid state drive - external (portable)</p> </div> <div data-bbox="525 1242 1795 1299"> <p>See https://www.dell.com/en-us/shop/sandisk-extreme-portable-solid-state-drive-500-gb-external-portable-usb-31-gen-2/apd/ab609642/storage-drives-media</p> </div> <div data-bbox="525 1315 1024 1347"> <p>Below are examples of Western Digital SSDs:</p> </div> |

Exhibit A-1 to Greenthread's Complaint













| U.S. Patent No. 10,510,842 | Accused Products |
|----------------------------|---|
| | <div data-bbox="703 207 1045 1279"> <p>Is this relevant?   </p> <p><input type="checkbox"/> Compare</p>  <p>WD Blue 3D NAND SATA SSD WDS200T2B0A - Solid state drive - 2 TB - internal - 2.5-inch - SATA 6Gb/s</p> <p>Estimated Value \$269.99 \$229.99 You Save \$40.00 (15%)</p> <p>Get it as soon as Monday, May 2 View Delivery Dates for 20170</p> <p>Manufacturer Part WDS200T2B0A Dell Part A9935209</p> <p>View Details</p> </div> <div data-bbox="1077 207 1419 1279"> <p>Is this relevant?   </p> <p><input type="checkbox"/> Compare</p>  <p>WD Blue 3D NAND SATA SSD WDS200T2B0B - Solid state drive - 2 TB - internal - M.2 2280 - SATA 6Gb/s</p> <p>Estimated Value \$263.99 \$243.99 You Save \$20.00 (8%)</p> <p>Get it as soon as Monday, May 2 View Delivery Dates for 20170</p> <p>Manufacturer Part WDS200T2B0B Dell Part A9935210</p> <p>View Details</p> </div> <div data-bbox="1451 207 1793 1279"> <p>Is this relevant?   </p> <p><input type="checkbox"/> Compare</p>  <p>WD Blue 3D NAND SATA SSD WDS100T2B0B - Solid state drive - 1 TB - internal - M.2 2280 - SATA 6Gb/s</p> <p>★★★★★ 4.6 (17)</p> <p>Estimated Value \$129.99 \$117.99 You Save \$12.00 (9%)</p> <p>Get it as soon as Monday, May 2 View Delivery Dates for 20170</p> <p>Manufacturer Part WDS100T2B0B Dell Part A9935211</p> <p>View Details</p> </div> <div data-bbox="1785 438 1827 592" style="writing-mode: vertical-rl; transform: rotate(180deg);">Call or Chat</div> <p>See https://www.dell.com/en-us/search/wd%20ssd%20blue%203d</p> <p>Such SSDs, like the other flash memory devices (e.g., SD/microSD cards), are semiconductor devices.</p> |

Exhibit A-1 to Greenthread's Complaint

| U.S. Patent No. 10,510,842 | Accused Products |
|---|--|
| | <p>What is a flash solid-state drive (SSD)?</p> <p>A flash solid-state drive (SSD) is a non-volatile storage device that stores persistent data in flash memory. There are two types of flash memory used in SSDs -- NAND and NOR.</p> <p>See https://www.techtarget.com/searchstorage/definition/flash-based-solid-state-drive-SSD</p> <p>Solid state refers to electronic circuitry that is built entirely of semiconductors. The term was originally used to define those electronics, such as a transistor radio that used semiconductors rather than vacuum tubes in its construction.</p> <p>Most electronics today are built around semiconductors and chips. A solid state drive uses, as its primary storage medium, semiconductors rather than the magnetic platters of a conventional hard drive.</p> <p>See https://www.lifewire.com/solid-state-drive-833448</p> <p>The above SanDisk flash memory card and the above SanDisk and Western Digital SSDs are representative examples of the Western Digital Accused Products, e.g., because all of these devices include a flash memory.</p> <p>A SanDisk 15 nm node NAND flash memory has been analyzed via tear-down and is described in this claim chart and other infringement contention claim charts (e.g., Exhibits A-1 through A-6), as explained below, as a representative example of the Western Digital Accused Products. Upon information and belief, other flash memory devices would have similarly been advantageously designed to move carriers (e.g., towards the substrate) and achieve the performance enhancements described and claimed in the '842 patent (and the other asserted patents). For example, other flash memory devices would similarly have been designed with a dopant gradient in order to improve performance characteristics such as on and off switching times and other performance enhancements described in the Abstract of the '842 patent (and the other asserted patents). Therefore, upon information and belief, other Western Digital Accused Products contain similar features as the SanDisk 15 nm node NAND flash memory, and function in a similar way, with respect to the features claimed in the asserted claims.</p> <p>This claim chart is based on publicly available information, and additional information regarding these and other accused products is expected to be obtained through discovery.</p> |
| <p>[Claim 1, Element 1] a substrate of a first doping type at a first doping level having first and second surfaces;</p> | <p>The Western Digital Accused Products include a semiconductor device comprising a substrate of a first doping type at a first doping level having first and second surfaces. For example, a die of the SanDisk flash memory discussed above for the preamble is shown below:</p> |

Exhibit A-1 to Greenthread's Complaint

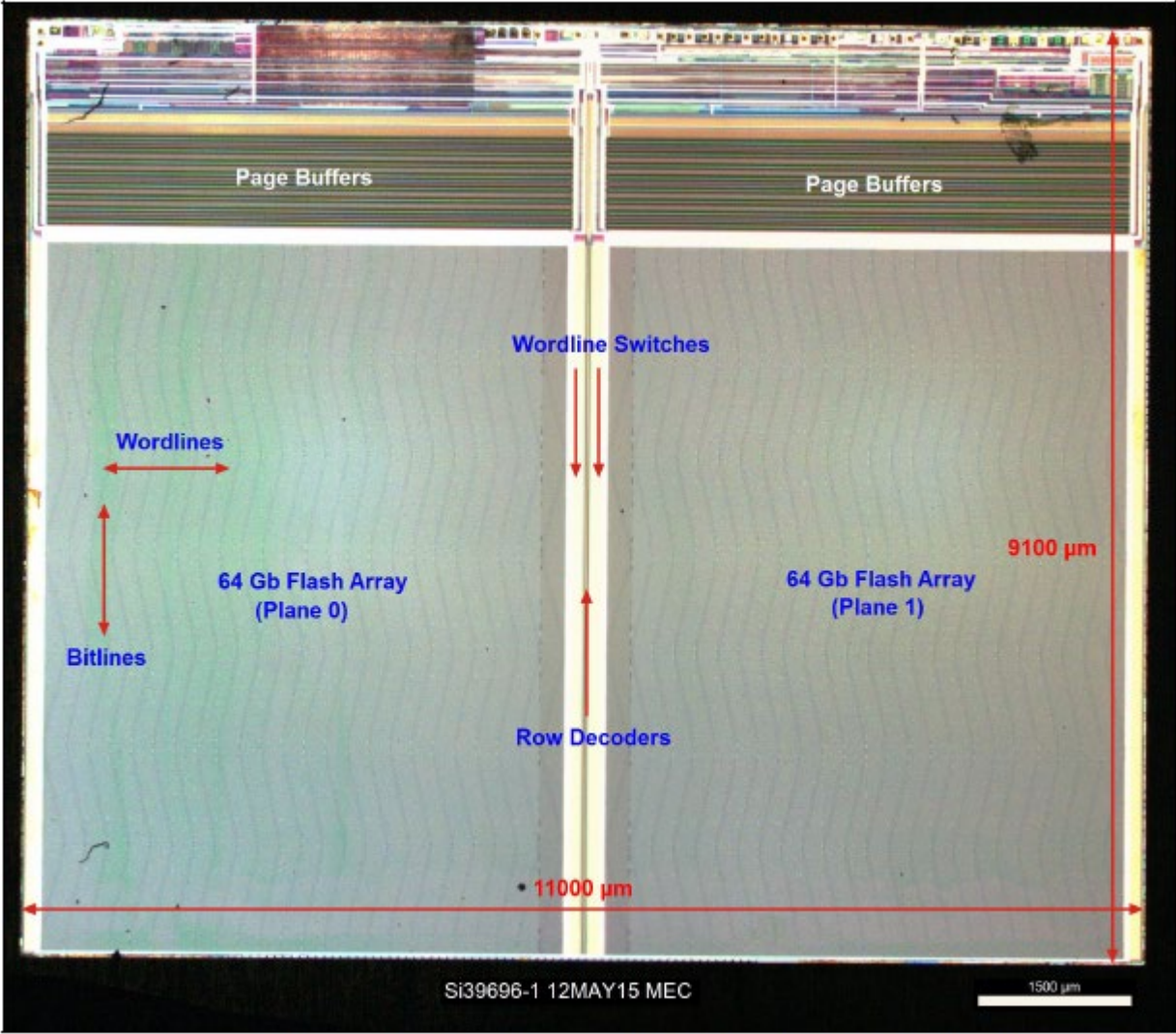
| U.S. Patent No. 10,510,842 | Accused Products |
|----------------------------|--|
| |  <p>The die photograph shows a rectangular silicon die with a central vertical strip. The die is divided into two main sections: the left section is labeled '64 Gb Flash Array (Plane 0)' and the right section is labeled '64 Gb Flash Array (Plane 1)'. The top edge of the die features two 'Page Buffers'. The central vertical strip contains 'Wordline Switches' and 'Row Decoders'. The left section also shows 'Wordlines' and 'Bitlines'. Dimensions are indicated: a horizontal dimension of 11000 μm and a vertical dimension of 9100 μm. A scale bar at the bottom right indicates 1500 μm. The text 'Si39696-1 12MAY15 MEC' is visible at the bottom center of the die.</p> <p>Figure 1.2.1: Die photograph of Toshiba/SanDisk 16 GB NAND die</p> |

Exhibit A-1 to Greenthread's Complaint

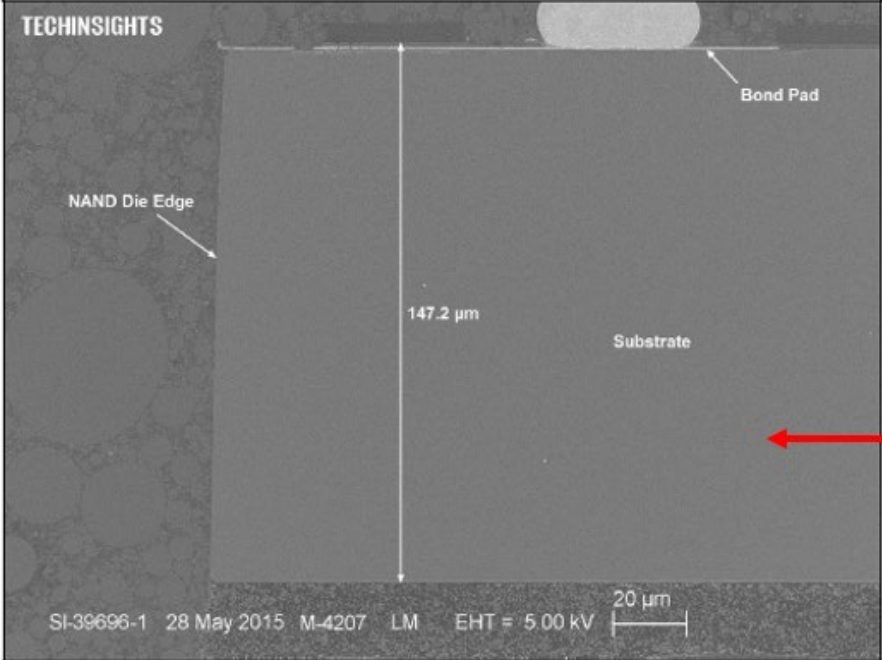
| U.S. Patent No. 10,510,842 | Accused Products |
|----------------------------|--|
| | <p>The following image of a cross-section of the flash memory die, obtained through scanning electron microscopy (SEM), shows the die having a thickness of 147.2 μm in this example. The flash memory die includes a substrate having first and second surfaces, as shown below:</p>  <p style="text-align: center;">Figure 1.2.3: Die thickness, SEM cross-sectional image</p> <p>A thickness (depth) of, e.g., 147.2 μm is consistent with the presence of a substrate.</p> <p>Spreading resistance profile (SRP) analysis conducted on the flash memory shows that the substrate is p-type (a first doping type) and has a first doping level (see concentration of p-type substrate in below graph).</p> |

Exhibit A-1 to Greenthread's Complaint

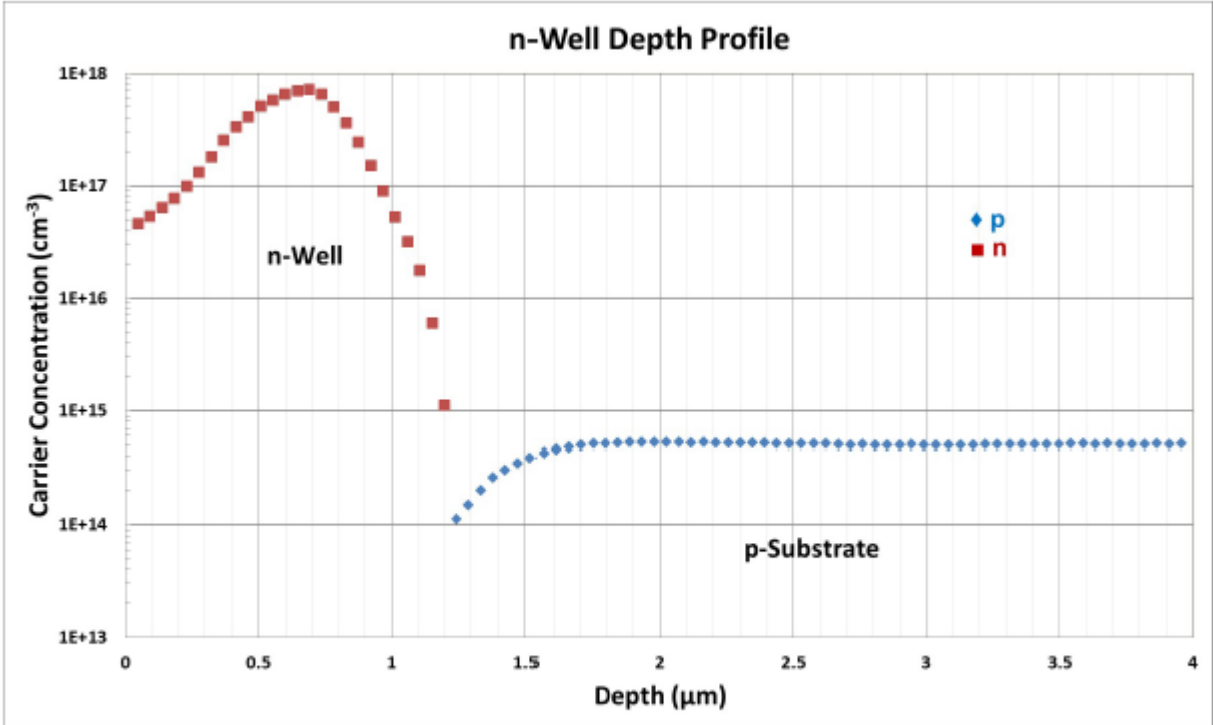
| U.S. Patent No. 10,510,842 | Accused Products |
|---|--|
| |  <p data-bbox="898 961 1625 1029">Figure 2.1.4: Periphery n-well in p-doped Si substrate, spreading resistance profile</p> |
| <p data-bbox="109 1081 499 1292">[Claim 1, Element 2] a first active region disposed adjacent the first surface of the substrate with a second doping type opposite in conductivity to the first doping type and within which transistors can be formed;</p> | <p data-bbox="529 1081 1986 1201">The Western Digital Accused Products include a semiconductor device comprising a first active region disposed adjacent the first surface of the substrate with a second doping type opposite in conductivity to the first doping type and within which transistors can be formed. For example, the following cross-sectional image (labeled Figure 2.3.5) of the SanDisk flash memory device discussed above, obtained through scanning electron microscopy (SEM), shows a first active region as claimed:</p> |

Exhibit A-1 to Greenthread's Complaint

| U.S. Patent No. 10,510,842 | Accused Products |
|----------------------------|--|
| | <div data-bbox="604 224 1852 971"> </div> <p data-bbox="814 990 1900 1026">Figure 2.3.5: LV logic PMOS transistors, SEM cross-sectional image with Si etch</p> <p data-bbox="529 1058 1978 1149">A PMOS transistor is shown above the first active region, and thus the first active region is a region within which transistors can be formed. For example, the gate of such a transistor is labeled in the above image. As shown in the above image, the first active region is disposed adjacent the first surface of the substrate.</p> <p data-bbox="529 1166 1978 1256">The first active region has a second doping type (e.g., n-type) opposite in conductivity to the first doping type (p-type), e.g., as PMOS transistors are formed in n-wells. The presence of P⁺ diffusion regions to the left and right of the first active region is consistent with the presence of PMOS transistors. The n-type doping of the n-well is also shown in the following SRP graph.</p> |

Exhibit A-1 to Greenthread's Complaint

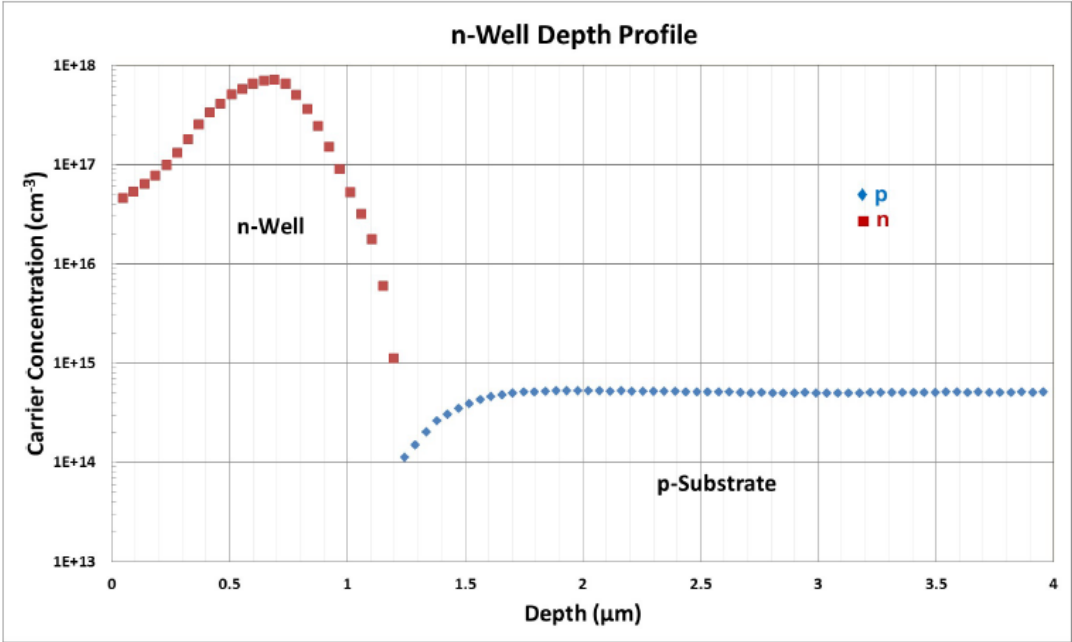
| U.S. Patent No. 10,510,842 | Accused Products |
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| |  <p data-bbox="934 868 1585 933">Figure 2.1.4: Periphery n-well in p-doped Si substrate, spreading resistance profile</p> <p data-bbox="529 966 1297 998">The n-well shown above contains the first active region which is n-type.</p> |
| <p data-bbox="109 1031 499 1177">[Claim 1, Element 3] a second active region separate from the first active region disposed adjacent to the first active region and within which transistors can be formed;</p> | <p data-bbox="529 1031 1990 1128">The Western Digital Accused Products include a semiconductor device comprising a second active region separate from the first active region disposed adjacent to the first active region and within which transistors can be formed. For example, a second active region as claimed is shown in the below SEM image (labeled Figure 2.3.4):</p> |

Exhibit A-1 to Greenthread's Complaint

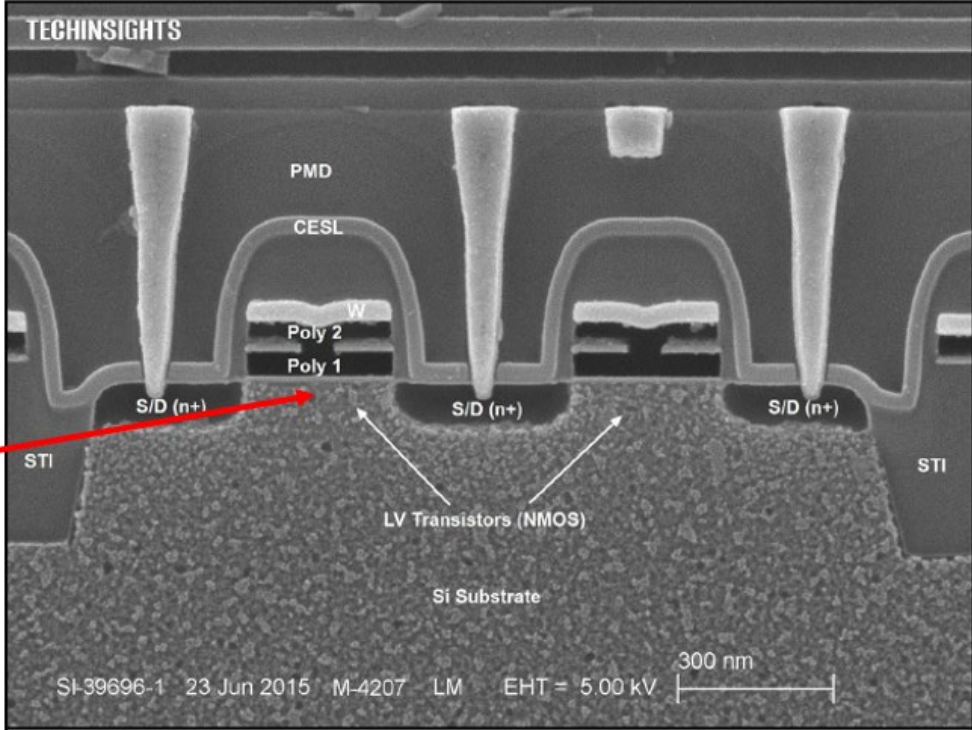
| U.S. Patent No. 10,510,842 | Accused Products |
|----------------------------|---|
| |  <p data-bbox="879 971 1940 1003">Figure 2.3.4: LV logic NMOS transistors, SEM cross-sectional image with Si etch</p> <p data-bbox="527 1024 1976 1081">An NMOS transistor is shown above the second active region, and thus the second active region is a region within which transistors can be formed. For example, the gate of such a transistor is labeled in the above image.</p> |

Exhibit A-1 to Greenthread's Complaint

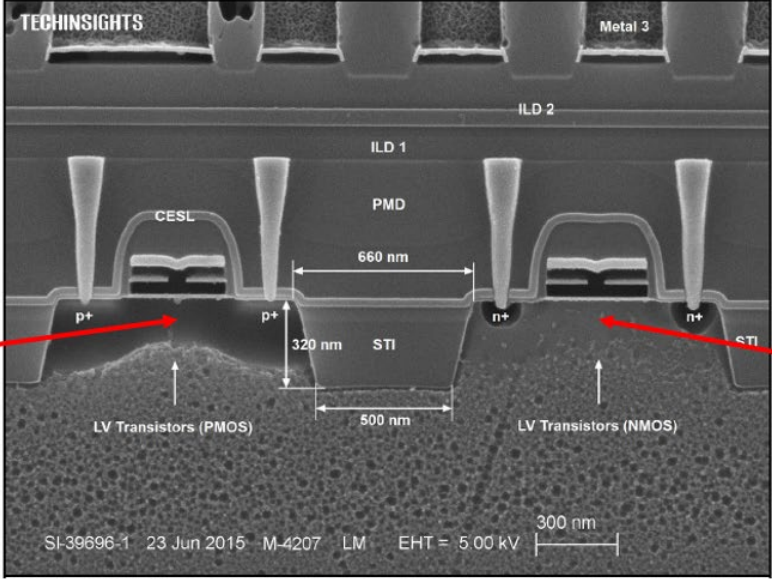
| U.S. Patent No. 10,510,842 | Accused Products |
|---|---|
| |  <p data-bbox="961 813 1549 865">Figure 2.3.9: LV logic NMOS and PMOS transistor, SEM cross-sectional image with Si etch</p> <p data-bbox="527 899 1898 956">As shown in the above SEM image (labeled Figure 2.3.9), the second active region (which is shown near an NMOS transistor) is separate from the first active region (which is shown near a PMOS transistor) and is disposed adjacent to the first active region.</p> |
| <p data-bbox="107 992 464 1114">[Claim 1, Element 4] transistors formed in at least one of the first active region or second active region; and</p> | <p data-bbox="527 979 1992 1036">The Western Digital Accused Products include a semiconductor device comprising transistors formed in at least one of the first active region or second active region. <i>See</i> above at Elements 2-3.</p> |
| <p data-bbox="107 1149 491 1360">[Claim 1, Element 5] at least a portion of at least one of the first and second active regions having at least one graded dopant concentration to aid carrier movement from the first surface to the second surface of the substrate.</p> | <p data-bbox="527 1136 1969 1463">The Western Digital Accused Products include a semiconductor device comprising at least a portion of at least one of the first and second active regions having at least one graded dopant concentration to aid carrier movement from the first surface to the second surface of the substrate. For example, spreading resistance profiling (SRP) analysis shows a graded dopant concentration, as explained below. SRP and SIMS are well-known methods of studying semiconductor devices. <i>See e.g.</i>, T. Clarysse, et al. <i>Characterization of electrically active dopant profiles with the spreading resistance probe</i>, Materials Science and Engineering (December 2004). SRP provides an “electrical depth profile” and “gives intrinsically electrical information.” <i>Id.</i> at 141, 157. Each SRP data point reflects carrier movement and dopant concentration at the physical location at which it was taken. The plots of SRP data taken from accused products shown herein demonstrate differences in carrier concentration as a function of depth, which generate electric fields within the accused products. That is the SRP plots included in Greenthread’s infringement charts evidence both dopant gradients and the corresponding vertical electric drift fields. A silicon sample may be polished at an angle toward the top surface, and a defined profile may be generated over the depth of the sample via the grinding angle. The polished section was then electrically characterized using a</p> |

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| U.S. Patent No. 10,510,842 | Accused Products |
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| | <p>step probe, which generated a depth profile. For example, the graphs below, obtained via SRP analysis electrically characterizing the Western Digital Accused Products, show a graded dopant concentration (annotated with green oval) in the first active region (e.g., as shown by the concentration corresponding to an n-well in the first graph below) and in the second active region (e.g., as shown by the concentration corresponding to a p-well in the second graph below) to aid carrier movement from the first surface to the second surface of the substrate (e.g., downwards, corresponding to increasing depth, in the below graphs).</p> <div data-bbox="642 386 1869 1120"> </div> <p>Figure 2.1.4: Periphery n-well in p-doped Si substrate, spreading resistance profile</p> |

Exhibit A-1 to Greenthread's Complaint

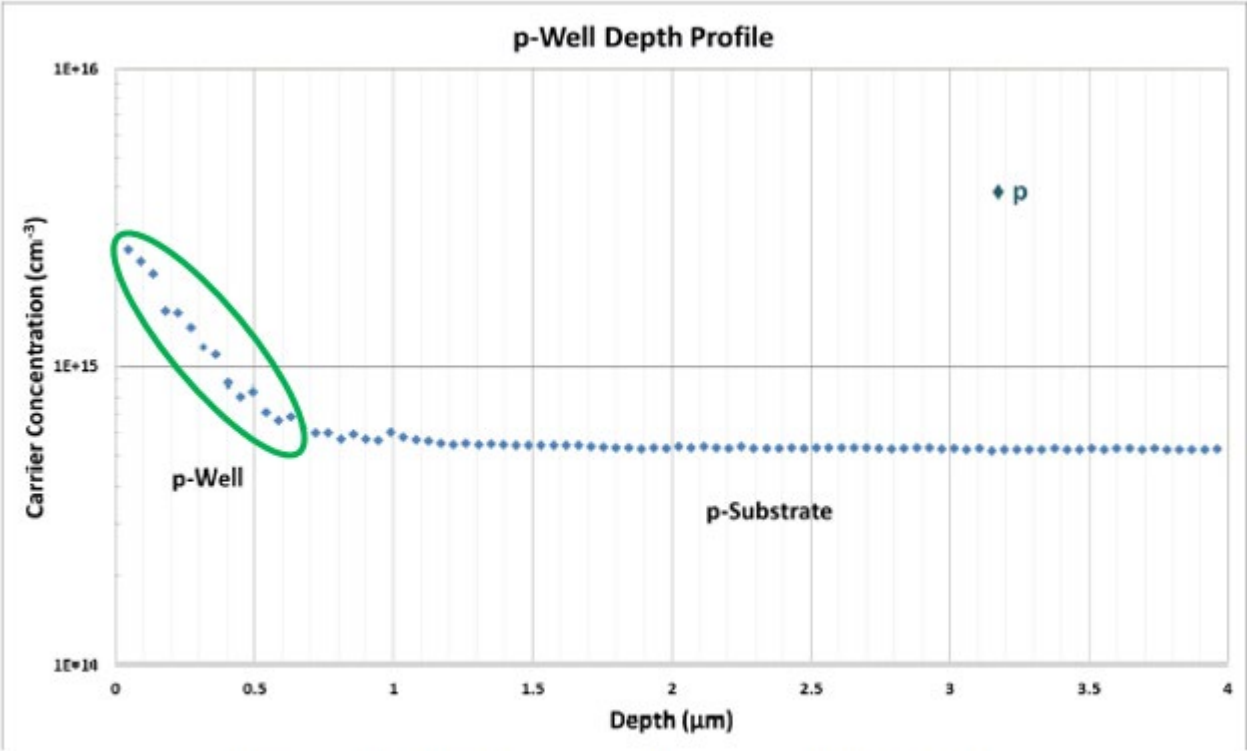
| U.S. Patent No. 10,510,842 | Accused Products |
|---|---|
| |  <p data-bbox="882 974 1638 1047">Figure 2.1.5: Periphery p-well in n-doped Si substrate, spreading resistance profile</p> |
| 2. The semiconductor device of claim 1, wherein the substrate is a p-type substrate. | The substrate of the semiconductor device of the Western Digital Accused Products is a p-type substrate, as discussed above for Claim 1, Element 1. |
| 4. The semiconductor device of claim 1, wherein the substrate has epitaxial silicon on top of a nonepitaxial substrate. | The substrate of the semiconductor device of the Western Digital Accused Products has epitaxial silicon on top of a nonepitaxial substrate. Upon information and belief, the substrate used in the Western Digital Accused Products is a single-crystal silicon wafer. Additionally, SRP analysis shows a curve downwards in the below blue (corresponding to substrate) plot (from 1.7 μm towards shallower depths) indicative of a purer layer grown on the substrate, and this is likely implemented via epitaxy. |

Exhibit A-1 to Greenthread's Complaint

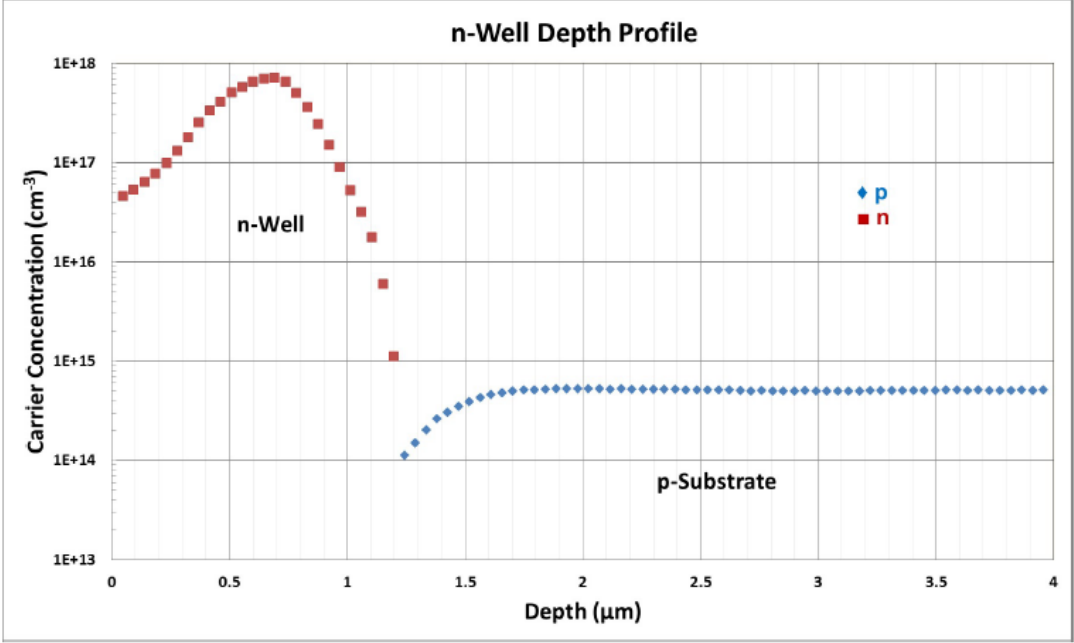
| U.S. Patent No. 10,510,842 | Accused Products |
|--|--|
| |  <p>The graph, titled "n-Well Depth Profile", plots Carrier Concentration (cm⁻³) on a logarithmic y-axis (from 1E+13 to 1E+18) against Depth (μm) on a linear x-axis (from 0 to 4). Red squares represent the n-well concentration, which rises from ~1E+16 at 0 μm to a peak of ~1E+18 at 0.7 μm, then drops sharply. Blue diamonds represent the p-substrate concentration, which remains low (~1E+14) until ~1.2 μm, then rises to a plateau of ~1E+14.5 for depths greater than 1.5 μm. Labels "n-Well" and "p-Substrate" are placed near their respective curves. A legend in the top right shows a blue diamond for "p" and a red square for "n".</p> <p>Figure 2.1.4: Periphery n-well in p-doped Si substrate, spreading resistance profile</p> |
| <p>5. The semiconductor device of claim 1, wherein the first active region and second active region contain one of either p-channel and n-channel devices.</p> | <p>The Western Digital Accused Products meet this limitation. For example, in the following SEM image, the first and second active regions correspond to PMOS and NMOS transistors, respectively, e.g., as shown in the following SEM images (labeled Figures 2.3.14 and 2.3.15; <i>see also</i> above at Claim 1, Elements 2-3).</p> |

Exhibit A-1 to Greenthread's Complaint

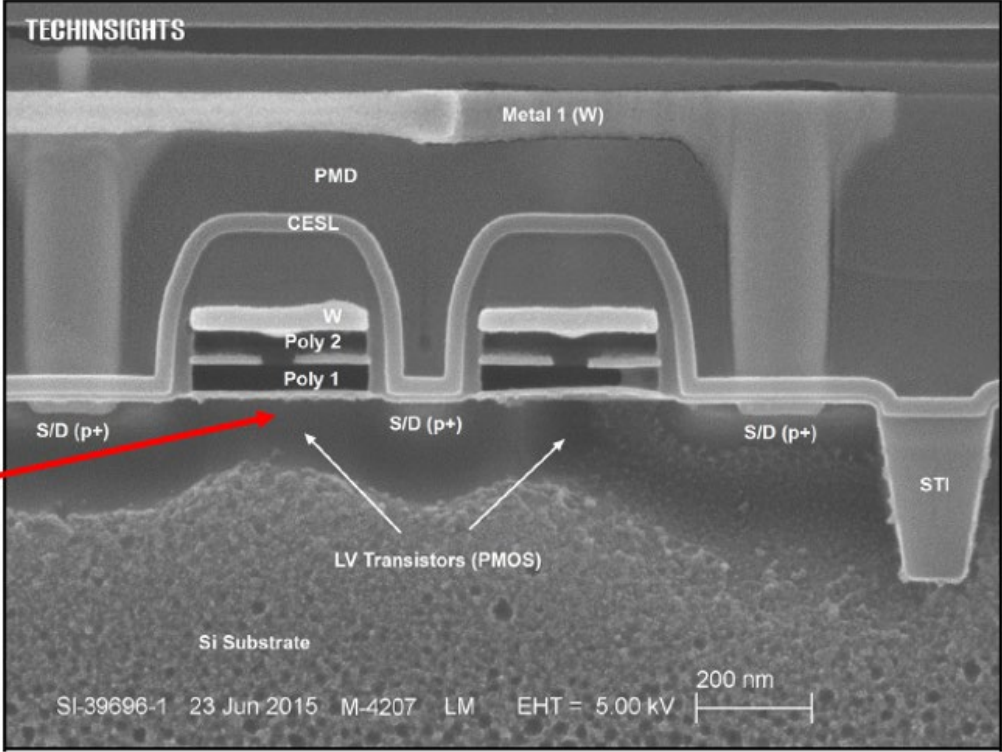
| U.S. Patent No. 10,510,842 | Accused Products |
|----------------------------|---|
| | <div data-bbox="548 670 716 751">first active region</div> <div data-bbox="806 224 1801 971"><p>TECHINSIGHTS</p><p>Metal 1 (W)</p><p>PMD</p><p>CESL</p><p>W</p><p>Poly 2</p><p>Poly 1</p><p>S/D (p+)</p><p>LV Transistors (PMOS)</p><p>Si Substrate</p><p>STI</p><p>SI-39696-1 23 Jun 2015 M-4207 LM EHT = 5.00 kV 200 nm</p><p>Detailed description: This is a scanning electron micrograph (SEM) cross-section of a semiconductor device. The image shows a silicon (Si) substrate at the base. On top of the substrate, there are two PMOS transistors. The gate stack for each transistor consists of a polysilicon layer (Poly 1) and a tungsten (W) layer. Above the gate stack is a conductive overlayer (CESL). The transistors are separated by a shallow trench isolation (STI) region. The source and drain regions are labeled S/D (p+). A red arrow points to the first active region, which is the area where the transistor is formed. The image includes a scale bar of 200 nm and technical data at the bottom: SI-39696-1, 23 Jun 2015, M-4207, LM, EHT = 5.00 kV.</p></div> <p data-bbox="762 992 1848 1024">Figure 2.3.5: LV logic PMOS transistors, SEM cross-sectional image with Si etch</p> |

Exhibit A-1 to Greenthread's Complaint

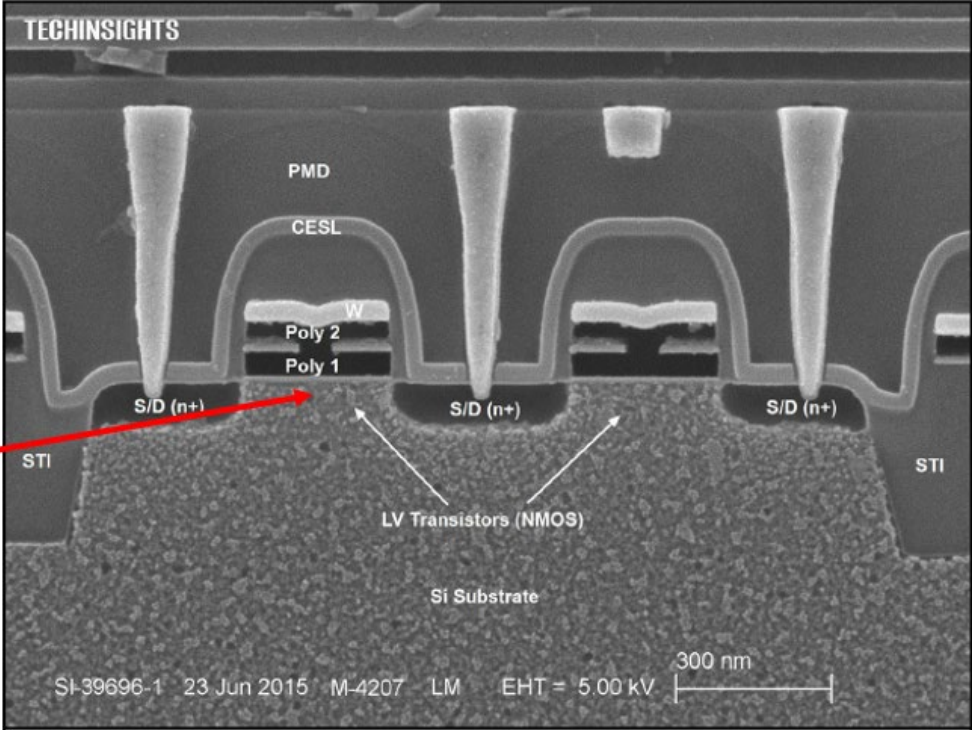
| U.S. Patent No. 10,510,842 | Accused Products |
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| |  <p data-bbox="533 659 743 737">second active region</p> <p data-bbox="842 972 1902 1005">Figure 2.3.4: LV logic NMOS transistors, SEM cross-sectional image with Si etch</p> <p data-bbox="527 1026 1990 1084">Thus, the first active region and second active region contain one of either p-channel and n-channel devices (e.g., the first active region contains a p-channel device, and the second active region contains an n-channel device).</p> |
| <p data-bbox="107 1122 468 1328">6. The semiconductor device of claim 1, wherein the first active region and second active region contain either p-channel or n-channel devices in n-wells or p-wells, respectively, and each well has a graded dopant.</p> | <p data-bbox="527 1105 1938 1224">The Western Digital Accused Products meet this limitation. As discussed above for Claim 5, the periphery (region with peripheral NMOS and PMOS transistors shown in Figures 2.3.4 and 2.3.5) contains NMOS (n-channel) and PMOS (p-channel) devices in respective p-wells and n-wells. As discussed above for Claim 1, Elements 2-3 and Claim 5, the p-channel and n-channel devices are contained in the first and active regions (<i>see</i> annotated Figures 2.3.4 and 2.3.5 discussed above).</p> <p data-bbox="527 1243 1986 1302">The following graphs obtained via SRP analysis show a p-well having a graded dopant (e.g., depths from 0 to about 0.8 μm in first graph below) and an n-well having a graded dopant (e.g., depths of about 0.7-1.2 μm in second graph below).</p> |

Exhibit A-1 to Greenthread's Complaint

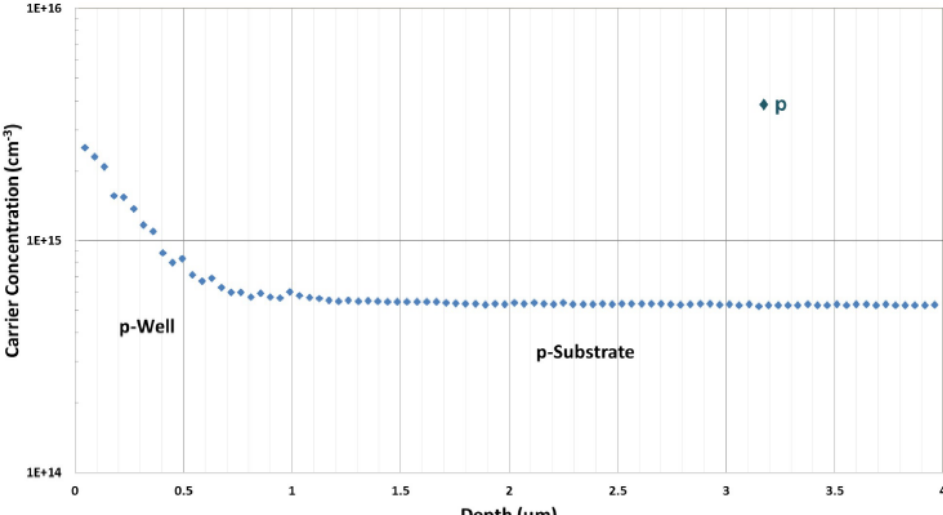
| U.S. Patent No. 10,510,842 | Accused Products | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
|----------------------------|--|------------|------------------------------|-----|---------|-----|---------|-----|---------|-----|---------|-----|---------|-----|---------|-----|---------|-----|---------|-----|---------|-----|---------|-----|-----------------------|-----|---------|-----|---------|
| | <div data-bbox="772 199 1738 776"><p style="text-align: center;">p-Well Depth Profile</p><table border="1"><caption>Approximate data points from Figure 2.1.5</caption><thead><tr><th>Depth (μm)</th><th>Carrier Concentration (cm⁻³)</th></tr></thead><tbody><tr><td>0.0</td><td>3.0E+15</td></tr><tr><td>0.2</td><td>1.5E+15</td></tr><tr><td>0.4</td><td>8.0E+14</td></tr><tr><td>0.6</td><td>5.0E+14</td></tr><tr><td>0.8</td><td>4.0E+14</td></tr><tr><td>1.0</td><td>3.5E+14</td></tr><tr><td>1.5</td><td>3.0E+14</td></tr><tr><td>2.0</td><td>3.0E+14</td></tr><tr><td>2.5</td><td>3.0E+14</td></tr><tr><td>3.0</td><td>3.0E+14</td></tr><tr><td>3.2</td><td>3.0E+15 (labeled 'p')</td></tr><tr><td>3.5</td><td>3.0E+14</td></tr><tr><td>4.0</td><td>3.0E+14</td></tr></tbody></table></div> <p style="text-align: center;">Figure 2.1.5: Periphery p-well in n-doped Si substrate, spreading resistance profile</p> | Depth (μm) | Carrier Concentration (cm⁻³) | 0.0 | 3.0E+15 | 0.2 | 1.5E+15 | 0.4 | 8.0E+14 | 0.6 | 5.0E+14 | 0.8 | 4.0E+14 | 1.0 | 3.5E+14 | 1.5 | 3.0E+14 | 2.0 | 3.0E+14 | 2.5 | 3.0E+14 | 3.0 | 3.0E+14 | 3.2 | 3.0E+15 (labeled 'p') | 3.5 | 3.0E+14 | 4.0 | 3.0E+14 |
| Depth (μm) | Carrier Concentration (cm⁻³) | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| 0.0 | 3.0E+15 | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| 0.2 | 1.5E+15 | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| 0.4 | 8.0E+14 | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| 0.6 | 5.0E+14 | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| 0.8 | 4.0E+14 | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| 1.0 | 3.5E+14 | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| 1.5 | 3.0E+14 | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| 2.0 | 3.0E+14 | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| 2.5 | 3.0E+14 | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| 3.0 | 3.0E+14 | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| 3.2 | 3.0E+15 (labeled 'p') | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| 3.5 | 3.0E+14 | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| 4.0 | 3.0E+14 | | | | | | | | | | | | | | | | | | | | | | | | | | | | |

Exhibit A-1 to Greenthread's Complaint

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| | <div data-bbox="772 212 1743 792" data-label="Figure"> </div> <p data-bbox="961 808 1554 865">Figure 2.1.4: Periphery n-well in p-doped Si substrate, spreading resistance profile</p> <p data-bbox="527 901 1990 961">The first and second active regions contain either p-channel or n-channel devices in these n-wells/p-wells because in CMOS technology a p-channel device is formed in an n-well and an n-channel device is formed in a p-well.</p> |
| 7. The semiconductor device of claim 1, wherein the first active region and second active region are each separated by at least one isolation region. | <p data-bbox="527 982 1990 1068">The Western Digital Accused Products meet this limitation. The following SEM cross-sectional image shows that the first active region and second active region are each separated by at least one isolation region, which is a shallow-trench isolation as indicated by the label STI (annotated below with red oval).</p> |

Exhibit A-1 to Greenthread's Complaint

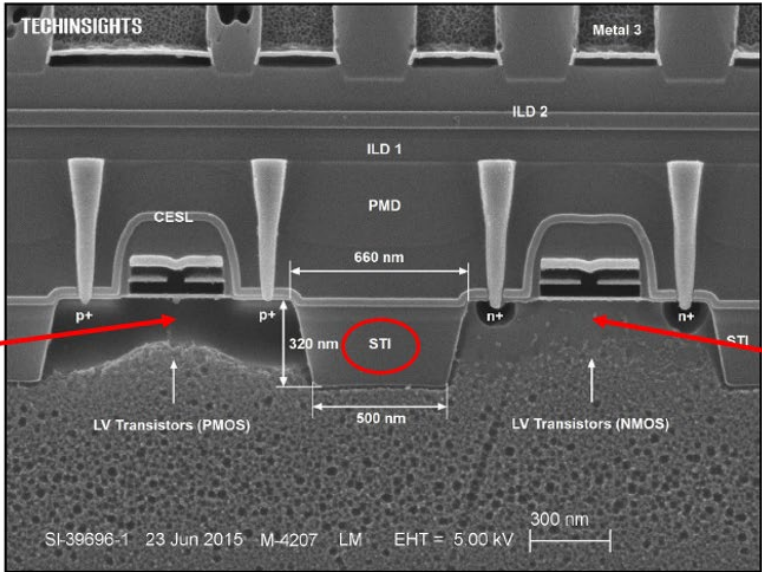
| U.S. Patent No. 10,510,842 | Accused Products |
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| |  <p data-bbox="955 820 1543 868">Figure 2.3.9: LV logic NMOS and PMOS transistor, SEM cross-sectional image with Si etch</p> |
| 8. The semiconductor device of claim 1, wherein the graded dopant is fabricated with an ion implantation process. | Upon information and belief, the graded dopant is fabricated with an ion implantation process. For example, ion implantation is the prevalent process for implementing doping in semiconductor devices, and is believed to be used for the Western Digital Accused Products. Information about the fabrication process for Western Digital Accused Products, including usage of an ion implantation process, is in the possession of the Defendants and is expected to be obtained through discovery. |
| [Claim 9, Preamble] A semiconductor device, comprising: | To the extent the preamble is a limitation, the Western Digital Accused Products include a semiconductor device. <i>See</i> above at Claim 1, Preamble. |
| [Claim 9, Element 1] a substrate of a first doping type at a first doping level having first and second surfaces; | The Western Digital Accused Products meet this limitation. <i>See</i> above at Claim 1, Element 1. |
| [Claim 9, Element 2] a first active region disposed adjacent the first surface of the substrate with a second doping type opposite in | The Western Digital Accused Products meet this limitation. <i>See</i> above at Claim 1, Element 2. Upon information and belief, transistors can be formed in the surface of the first active region. Details regarding formation of transistors are in the possession of the Defendants and are expected to be obtained through discovery. |

Exhibit A-1 to Greenthread's Complaint

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| conductivity to the first doping type and within which transistors can be formed in the surface thereof; | |
| [Claim 9, Element 3] a second active region separate from the first active region disposed adjacent to the first active region and within which transistors can be formed in the surface thereof; | The Western Digital Accused Products meet this limitation. <i>See</i> above at Claim 1, Element 3. Upon information and belief, transistors can be formed in the surface of the second active region. Details regarding formation of transistors are in the possession of the Defendants and are expected to be obtained through discovery. |
| [Claim 9, Element 4] transistors formed in at least one of the first active region or second active region; and | The Western Digital Accused Products meet this limitation. <i>See</i> above at Claim 1, Element 4. |
| [Claim 9, Element 5] at least a portion of at least one of the first and second active regions having at least one graded dopant concentration to aid carrier movement from the surface to the substrate. | The Western Digital Accused Products meet this limitation. <i>See</i> above at Claim 1, Element 5 SRP analysis electrically characterizing the accused product and showing carrier movement and electric fields. SRP analysis generally is discussed at Claim 1, Element 5. |
| 10. The semiconductor device of claim 9, wherein the substrate is a p-type substrate. | The Western Digital Accused Products meet this limitation. <i>See</i> above at Claim 2. |
| 12. The semiconductor device of claim 9, wherein the substrate has epitaxial silicon on top of a nonepitaxial substrate. | The Western Digital Accused Products meet this limitation. <i>See</i> above at Claim 4. |
| 13. The semiconductor device of claim 9, wherein the first active region and second active region contain at least one of either p-channel and n-channel devices. | The Western Digital Accused Products meet this limitation. <i>See</i> above at Claim 5. |
| 14. The semiconductor device of claim 9, wherein the first active | The Western Digital Accused Products meet this limitation. <i>See</i> above at Claim 6. |

Exhibit A-1 to Greenthread's Complaint

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| region and second active region contain either p-channel or n-channel devices in n-wells or p-wells, respectively, and each well has a graded dopant. | |
| 15. The semiconductor device of claim 9, wherein the first active region and second active region are each separated by at least one isolation region. | Upon information and belief, the Western Digital Accused Products meet this limitation. <i>See</i> above at Claim 7. |
| 16. The semiconductor device of claim 9, wherein the graded dopant is fabricated with an ion implantation process. | Upon information and belief, the Western Digital Accused Products meet this limitation. <i>See</i> above at Claim 8. |
| 17. The semiconductor device of claim 1, wherein the first and second active regions are formed adjacent the first surface of the substrate. | The Western Digital Accused Products meet this limitation. <i>See</i> above at Claim 1, Elements 2-3. |
| 18. The semiconductor device of claim 1, wherein the transistors which can be formed in the first and second active regions are CMOS transistors requiring a source, a drain, a gate and a channel region. | The Western Digital Accused Products meet this limitation. <i>See</i> above at Claim 1, Elements 2-3; Claim 6. The SEM images labeled Figures 2.3.5 and 2.3.4 discussed above for Claim 1, Elements 2-3 and Claim 6 show NMOS and PMOS transistors, which are adjacent to one another as shown in the SEM image labeled Figure 2.3.9 discussed above for Claim 1, Element 3. Therefore, the transistors which can be formed in the first and second active regions are CMOS transistors. CMOS transistors require a source, a drain, a gate, and a channel region. The source and drain terminals of transistors are shown below, a gate is between each source-drain pair, and a channel region connects each source to a corresponding drain. |

Exhibit A-1 to Greenthread's Complaint

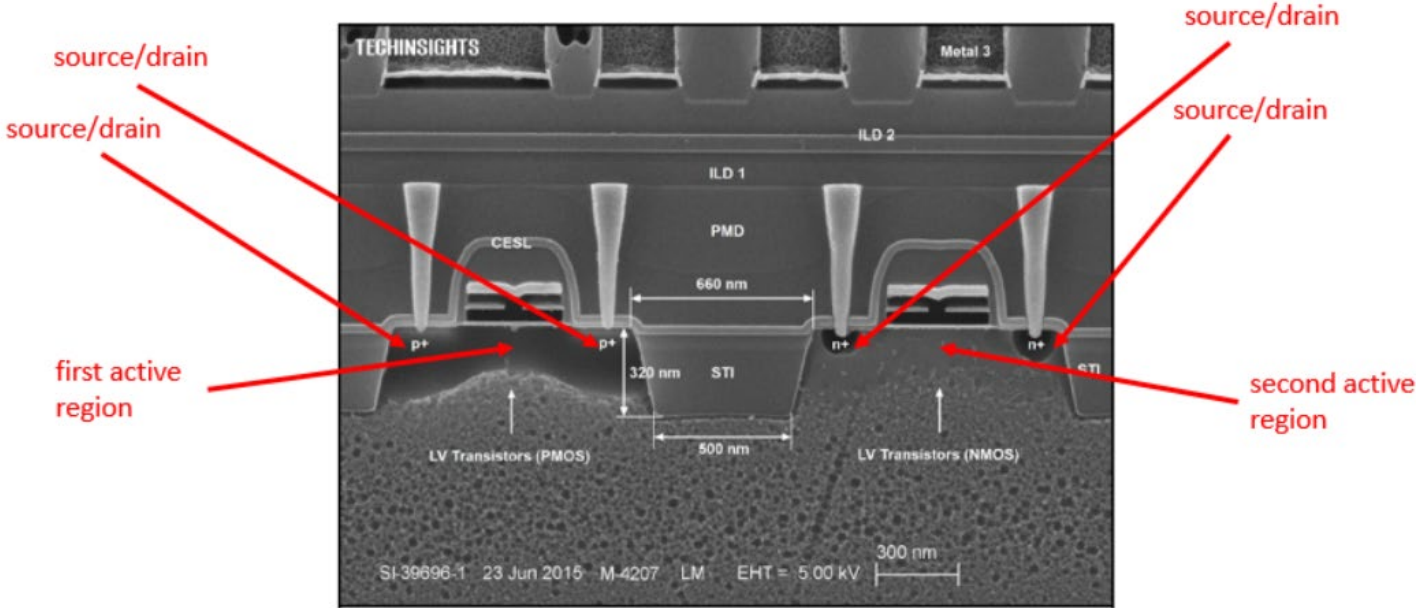
| U.S. Patent No. 10,510,842 | Accused Products |
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| |  <p>Figure 2.3.9: LV logic NMOS and PMOS transistor, SEM cross-sectional image with Si etch</p> |

Exhibit A-2 to Greenthread's Complaint

| U.S. Patent No. 10,734,481 | Accused Products |
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| <p>[Claim 1, Preamble] A semiconductor device, comprising:</p> | <p>To the extent the preamble is a limitation, the Western Digital Accused Products include a semiconductor device. <i>See</i> Exhibit A-1, Claim 1, Preamble. The SanDisk 15 nm 16 GB NAND flash memory referenced in Exhibit A-1 for tear-down analysis is discussed in this claim chart and other infringement contention claim charts as an example of a flash memory representative of the Western Digital Accused Products. Upon information and belief, such a SanDisk flash memory is representative of flash memory devices used in the Western Digital Accused Products for purposes of this claim chart and the other infringement contention claim charts because, e.g., other flash memory devices used in Western Digital Accused Products would have similarly been advantageously designed to move carriers (e.g., towards the substrate) and achieve the performance enhancements described and claimed in the '481 patent (and the other asserted patents). For example, other flash memory devices would similarly have been designed with a dopant gradient in order to improve performance characteristics such as on and off switching times and other performance enhancements described in the Abstract of the '481 patent (and the other asserted patents). Therefore, upon information and belief, other flash memory devices used in Western Digital Accused Products contain similar features as the SanDisk 16 nm 16 GB NAND flash memory, and function in a similar way, with respect to the features claimed in the asserted claims.</p> <p>This claim chart is based on publicly available information, and additional information regarding these and other accused products is expected to be obtained through discovery.</p> |
| <p>[Claim 1, Element 1] a substrate of a first doping type at a first doping level having first and second surfaces;</p> | <p>The Western Digital Accused Products meet this limitation. <i>See</i> Exhibit A-1, Claim 1, Element 1.</p> |
| <p>[Claim 1, Element 2] a first active region disposed adjacent the first surface of the substrate with a second doping type opposite in conductivity to the first doping type and within which transistors can be formed;</p> | <p>The Western Digital Accused Products meet this limitation. <i>See</i> Exhibit A-1, Claim 1, Element 2.</p> |
| <p>[Claim 1, Element 3] a second active region separate from the first active region disposed adjacent to the first active region and within which transistors can be formed;</p> | <p>The Western Digital Accused Products meet this limitation. <i>See</i> Exhibit A-1, Claim 1, Element 3.</p> |
| <p>[Claim 1, Element 4] transistors formed in at least one of the first active region or second active region;</p> | <p>The Western Digital Accused Products meet this limitation. <i>See</i> Exhibit A-1, Claim 1, Element 4.</p> |

Exhibit A-2 to Greenthread's Complaint

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| <p>[Claim 1, Element 5] at least a portion of at least one of the first and second active regions having at least one graded dopant concentration to aid carrier movement from the first surface to the second surface of the substrate; and</p> | <p>The Western Digital Accused Products meet this limitation. <i>See</i> Exhibit A-1, Claim 1, Element 5 SRP analysis electrically characterizing the accused product and showing carrier movement and electric fields. SRP analysis generally is discussed at Exhibit A-1, Claim 1, Element 5.</p> |
| <p>[Claim 1, Element 6] at least one well region adjacent to the first or second active region containing at least one graded dopant region, the graded dopant region to aid carrier movement from the first surface to the second surface of the substrate.</p> | <p>The Western Digital Accused Products meet this limitation. For example, the SanDisk flash memory includes a p-well (first graph below) and an n-well (second graph below) having graded dopant regions.</p> <div data-bbox="806 561 1709 1102"> <p>The graph, titled 'p-Well Depth Profile', plots Carrier Concentration (cm⁻³) on a logarithmic y-axis (from 10¹⁴ to 10¹⁶) against Depth (μm) on a linear x-axis (from 0 to 4). The data points show a steep decline from 10¹⁶ cm⁻³ at the surface to a plateau of approximately 10^{14.5} cm⁻³ at a depth of 1 μm. This plateau continues to 4 μm. The initial steep region is labeled 'p-Well' and the subsequent flat region is labeled 'p-Substrate'.</p> </div> <p>Figure 2.1.5: Periphery p-well in n-doped Si substrate, spreading resistance profile</p> |

Exhibit A-2 to Greenthread's Complaint

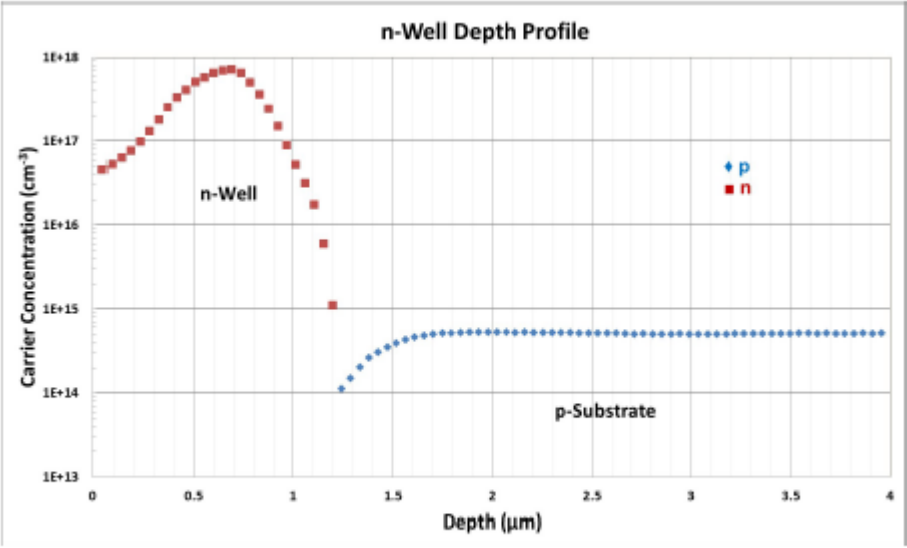
| U.S. Patent No. 10,734,481 | Accused Products |
|---|--|
| |  <p data-bbox="982 771 1528 824">Figure 2.1.4: Periphery n-well in p-doped Si substrate, spreading resistance profile</p> <p data-bbox="527 865 1990 922">These graded dopant regions are to aid carrier movement from the first surface to the second surface of the substrate. <i>See</i> Exhibit A-1, Claim 1, Element 5. SRP analysis generally is discussed at Exhibit A-1, Claim 1, Element 5.</p> |
| 2. The semiconductor device of claim 1, wherein the substrate is a p-type substrate. | The Western Digital Accused Products meet this limitation. <i>See</i> Exhibit A-1, Claim 2. |
| 3. The semiconductor device of claim 1, wherein the substrate has epitaxial silicon on top of a nonepitaxial substrate. | The Western Digital Accused Products meet this limitation. <i>See</i> Exhibit A-1, Claim 4. |
| 4. The semiconductor device of claim 1, wherein the first active region and second active region contain one of either p-channel and n-channel devices. | The Western Digital Accused Products meet this limitation. <i>See</i> Exhibit A-1, Claim 5. |
| 5. The semiconductor device of claim 1, wherein the first active | The Western Digital Accused Products meet this limitation. <i>See</i> Exhibit A-1, Claim 6. |

Exhibit A-2 to Greenthread's Complaint

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| region and second active region contain either p-channel or n-channel devices in n-wells or p-wells, respectively, and each well has at least one graded dopant. | |
| 6. The semiconductor device of claim 1, wherein the first active region and second active region are each separated by at least one isolation region. | The Western Digital Accused Products meet this limitation. <i>See</i> Exhibit A-1, Claim 7. |
| 7. The semiconductor device of claim 1, wherein the graded dopant is fabricated with an ion implantation process. | The Western Digital Accused Products meet this limitation. <i>See</i> Exhibit A-1, Claim 8. |
| 8. The semiconductor device of claim 1, wherein the first and second active regions are formed adjacent the first surface of the substrate. | The Western Digital Accused Products meet this limitation. <i>See</i> Exhibit A-1, Claim 1, Elements 1-3. |
| 9. The semiconductor device of claim 1, wherein dopants of the graded dopant concentration in the first active region or the second active region are either p-type or n-type. | The Western Digital Accused Products meet this limitation. <i>See</i> Exhibit A-1, Claim 1, Element 5 (SRP analysis of Figures 2.1.4 and 2.1.5 (below) showing n-type doping and p-type doping, respectively, at graded dopant concentration). |

Exhibit A-2 to Greenthread's Complaint

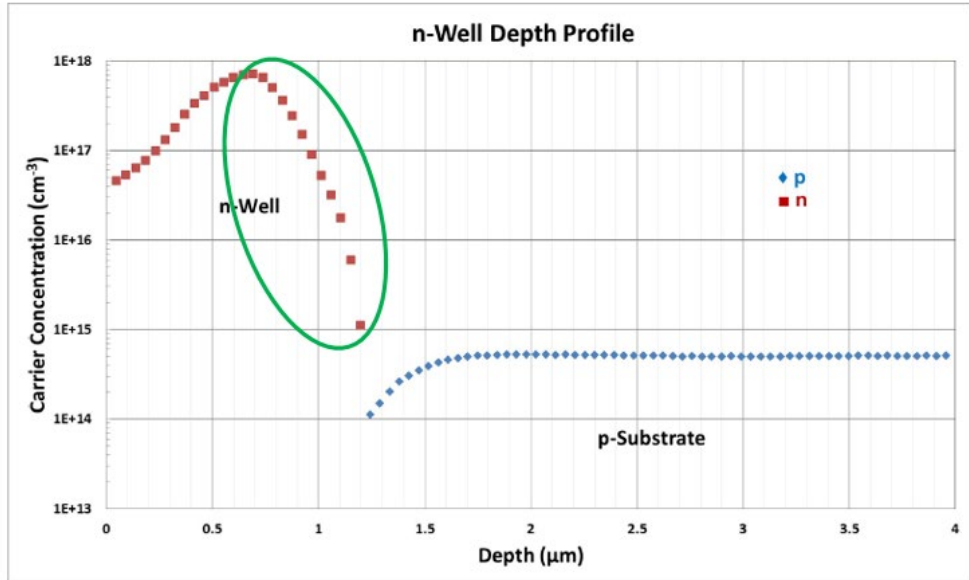
| U.S. Patent No. 10,734,481 | Accused Products | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
|----------------------------|--|---|--|---|-----|-------|---|-----|-------|---|-----|-------|---|-----|-------|---|-----|-------|-------|-----|---|-------|-----|---|-------|-----|---|-------|-----|---|-------|
| | <div><p style="text-align: center;">n-Well Depth Profile</p><p>The graph displays the carrier concentration profile for an n-well in a p-doped silicon substrate. The y-axis represents Carrier Concentration in cm⁻³ on a logarithmic scale from 1E+13 to 1E+18. The x-axis represents Depth in micrometers (μm) from 0 to 4. Red squares represent the n-well concentration, which starts at approximately 5E+16 cm⁻³ at the surface, peaks at about 8E+17 cm⁻³ at a depth of 0.7 μm, and then decays to 1E+15 cm⁻³ at 1.2 μm. A green oval highlights this n-well region. Blue diamonds represent the p-substrate concentration, which begins at 1.2 μm depth at approximately 1E+14 cm⁻³ and levels off to a constant value of about 5E+14 cm⁻³ from 1.8 μm onwards. The labels 'n-Well' and 'p-Substrate' are placed near their respective data series.</p><table><caption>Approximate data points from Figure 2.1.4</caption><tr><th>Depth (μm)</th><th>n-Well Carrier Concentration (cm⁻³)</th><th>p-Substrate Carrier Concentration (cm⁻³)</th></tr><tr><td>0.0</td><td>5E+16</td><td>-</td></tr><tr><td>0.5</td><td>1E+17</td><td>-</td></tr><tr><td>0.7</td><td>8E+17</td><td>-</td></tr><tr><td>1.0</td><td>1E+17</td><td>-</td></tr><tr><td>1.2</td><td>1E+15</td><td>1E+14</td></tr><tr><td>1.5</td><td>-</td><td>3E+14</td></tr><tr><td>2.0</td><td>-</td><td>5E+14</td></tr><tr><td>3.0</td><td>-</td><td>5E+14</td></tr><tr><td>4.0</td><td>-</td><td>5E+14</td></tr></table></div> <p style="text-align: center;">Figure 2.1.4: Periphery n-well in p-doped Si substrate, spreading resistance profile</p> | Depth (μm) | n-Well Carrier Concentration (cm ⁻³) | p-Substrate Carrier Concentration (cm ⁻³) | 0.0 | 5E+16 | - | 0.5 | 1E+17 | - | 0.7 | 8E+17 | - | 1.0 | 1E+17 | - | 1.2 | 1E+15 | 1E+14 | 1.5 | - | 3E+14 | 2.0 | - | 5E+14 | 3.0 | - | 5E+14 | 4.0 | - | 5E+14 |
| Depth (μm) | n-Well Carrier Concentration (cm ⁻³) | p-Substrate Carrier Concentration (cm ⁻³) | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| 0.0 | 5E+16 | - | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| 0.5 | 1E+17 | - | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| 0.7 | 8E+17 | - | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| 1.0 | 1E+17 | - | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| 1.2 | 1E+15 | 1E+14 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| 1.5 | - | 3E+14 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| 2.0 | - | 5E+14 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| 3.0 | - | 5E+14 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| 4.0 | - | 5E+14 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |

Exhibit A-2 to Greenthread's Complaint

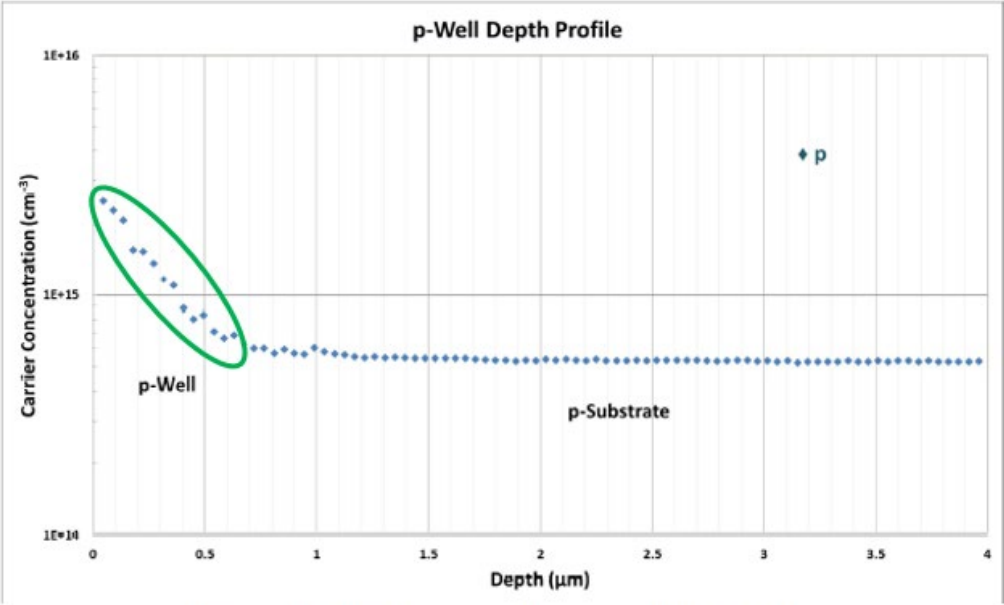
| U.S. Patent No. 10,734,481 | Accused Products |
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| |  <p data-bbox="961 824 1564 881">Figure 2.1.5: Periphery p-well in n-doped Si substrate, spreading resistance profile</p> |
| 13. The semiconductor device of claim 1, wherein the transistors which can be formed in the first and second active regions are CMOS transistors requiring at least a source, a drain, a gate and a channel. | The Western Digital Accused Products meet this limitation. <i>See</i> Exhibit A-1, Claim 18. |
| 15. The semiconductor device of claim 1, wherein the device is a complementary metal oxide semiconductor (CMOS) with a nonepitaxial substrate. | The Western Digital Accused Products meet this limitation. <i>See</i> Exhibit A-1, Claims 4 (regarding nonepitaxial substrate), 18 (regarding CMOS). |
| 16. The semiconductor device of claim 1, wherein the device is a flash memory. | The Western Digital Accused Products meet this limitation. <i>See</i> Exhibit A-1, Claim 1, Preamble. |

Exhibit A-2 to Greenthread's Complaint

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| [Claim 20, Preamble] A semiconductor device, comprising: | To the extent the preamble is a limitation, the Western Digital Accused Products meet include a semiconductor device. <i>See</i> above at Claim 1, Preamble. |
| [Claim 20, Element 1] a substrate of a first doping type at a first doping level having first and second surfaces; | The Western Digital Accused Products meet this limitation. <i>See</i> Exhibit A-1, Claim 1, Element 1. |
| [Claim 20, Element 2] a first active region disposed adjacent the first surface of the substrate with a second doping type opposite in conductivity to the first doping type and within which transistors can be formed in the surface thereof; | The Western Digital Accused Products meet this limitation. <i>See</i> Exhibit A-1, Claim 9, Element 2. |
| [Claim 20, Element 3] a second active region separate from the first active region disposed adjacent to the first active region and within which transistors can be formed in the surface thereof; | The Western Digital Accused Products meet this limitation. <i>See</i> Exhibit A-1, Claim 9, Element 3. |
| [Claim 20, Element 4] transistors formed in at least one of the first active region or second active region; | The Western Digital Accused Products meet this limitation. <i>See</i> Exhibit A-1, Claim 1, Element 4. |
| [Claim 20, Element 5] at least a portion of at least one of the first and second active regions having at least one graded dopant concentration to aid carrier movement from the surface to the substrate; and | The Western Digital Accused Products meet this limitation. <i>See</i> Exhibit A-1, Claim 1, Element 5. SRP analysis generally is discussed at Exhibit A-1, Claim 1, Element 5. |
| [Claim 20, Element 6] at least one well region adjacent to the first or second active region containing at least one graded dopant region, the graded dopant region to aid carrier | The Western Digital Accused Products meet this limitation. <i>See</i> above at Claim 1, Element 6. <i>See also</i> SRP analysis reproduced at Exhibit A-1 Claim 1 Element 5 electrically characterizing the accused product and showing carrier movement and electric fields. SRP analysis generally is discussed at Exhibit A-1, Claim 1, Element 5. |

Exhibit A-2 to Greenthread's Complaint

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| movement from the first surface to the second surface of the substrate. | |
| 22. The semiconductor device of claim 20, wherein the substrate is a p-type substrate. | The Western Digital Accused Products meet this limitation. <i>See</i> Exhibit A-1, Claim 2. |
| 23. The semiconductor device of claim 20, wherein the substrate has epitaxial silicon on top of a nonepitaxial substrate. | The Western Digital Accused Products meet this limitation. <i>See</i> Exhibit A-1, Claim 4. |
| 24. The semiconductor device of claim 20, wherein the first active region and second active region contain at least one of either p-channel and n-channel devices. | The Western Digital Accused Products meet this limitation. <i>See</i> Exhibit A-1, Claim 5. |
| 25. The semiconductor device of claim 20, wherein the first active region and second active region contain either p-channel or n-channel devices in n-wells or p-wells, respectively, and each well has at least one graded dopant. | The Western Digital Accused Products meet this limitation. <i>See</i> Exhibit A-1, Claim 6. |
| 26. The semiconductor device of claim 20, wherein the first active region and second active region are each separated by at least one isolation region. | The Western Digital Accused Products meet this limitation. <i>See</i> Exhibit A-1, Claim 7. |
| 27. The semiconductor device of claim 20, wherein dopants of the graded dopant concentration in the first active region or the second active region are either p-type or n-type. | The Western Digital Accused Products meet this limitation. <i>See</i> above at Claim 9. |

Exhibit A-2 to Greenthread's Complaint

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| 31. The semiconductor device of claim 20, wherein the graded dopant is fabricated with an ion implantation process. | The Western Digital Accused Products meet this limitation. <i>See</i> Exhibit A-1, Claim 8. |
| 32. The semiconductor device of claim 20, wherein the substrate is a complementary metal oxide semiconductor (CMOS) device. | The Western Digital Accused Products meet this limitation. <i>See</i> above at Claim 15. |
| 33. The semiconductor device of claim 20, wherein the device is a flash memory. | The Western Digital Accused Products meet this limitation. <i>See</i> above at Claim 16. |

Exhibit A-3 to Greenthread's Complaint

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| <p>[Claim 1, Preamble] A VLSI semiconductor device, comprising:</p> | <p>To the extent the preamble is a limitation, the Western Digital Accused Products include a VLSI semiconductor device. The SanDisk flash memory discussed for claim 1 of Exhibit A-1 is a semiconductor device (<i>see</i> Exhibit A-1, Claim 1, Preamble) with millions of transistors, and is a VLSI semiconductor device upon information and belief. Details regarding transistor count are in the possession of the Defendants and are expected to be obtained through discovery.</p> <p>The SanDisk 15 nm 16 GB NAND flash memory referenced in Exhibit A-1 is discussed in this claim chart and other infringement contention claim charts as an example of a flash memory representative of the Western Digital Accused Products. Upon information and belief, such a SanDisk flash memory is representative of flash memory devices used in the Western Digital Accused Products for purposes of this claim chart and the other infringement contention claim charts because, e.g., other flash memory devices used in Western Digital Accused Products would have similarly been advantageously designed to move carriers (e.g., towards the substrate) and achieve the performance enhancements described and claimed in the '222 patent (and the other asserted patents). For example, other flash memory devices would similarly have been designed with a dopant gradient in order to improve performance characteristics such as on and off switching times and other performance enhancements described in the Abstract of the '222 patent (and the other asserted patents). Therefore, upon information and belief, other flash memory devices used in Western Digital Accused Products contain similar features as the SanDisk 15 nm 16 GB NAND flash memory, and function in a similar way with respect to the features claimed in the asserted claims.</p> <p>This claim chart is based on publicly available information, and additional information regarding these and other accused products is expected to be obtained through discovery.</p> |
| <p>[Claim 1, Element 1] a substrate of a first doping type at a first doping level having a surface;</p> | <p>The Western Digital Accused Products meet this limitation. <i>See</i> Exhibit A-1, Claim 1, Element 1.</p> |

Exhibit A-3 to Greenthread's Complaint

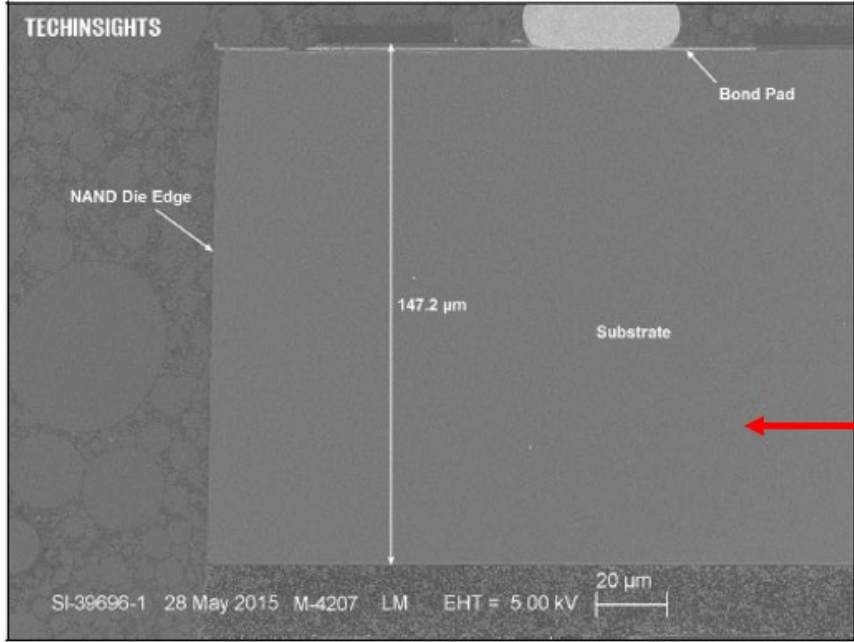
| U.S. Patent No. 11,121,222 | Accused Products |
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| |  <p>The image is a scanning electron micrograph (SEM) cross-section of a die. It shows a dark, textured 'Substrate' at the bottom and a lighter, smoother 'NAND Die Edge' on the left. A vertical white line with arrows at both ends indicates a thickness of '147.2 μm'. At the top right, a 'Bond Pad' is visible. A red arrow points to the top surface, labeled 'surface', and another red arrow points to the substrate, labeled 'substrate'. The top left corner of the image has the text 'TECHINSIGHTS'. The bottom of the image contains technical data: 'SI-39696-1 28 May 2015 M-4207 LM EHT = 5.00 kV' and a scale bar for '20 μm'.</p> <p>Figure 1.2.3: Die thickness, SEM cross-sectional image</p> |
| <p>[Claim 1, Element 2] a first active region disposed adjacent the surface with a second doping type opposite in conductivity to the first doping type and within which transistors can be formed;</p> | <p>The Western Digital Accused Products meet this limitation. <i>See</i> Exhibit A-1, Claim 1, Element 2.</p> |
| <p>[Claim 1, Element 3] a second active region separate from the first active region disposed adjacent to the first active region and within which transistors can be formed;</p> | <p>The Western Digital Accused Products meet this limitation. <i>See</i> Exhibit A-1, Claim 1, Element 3.</p> |

Exhibit A-3 to Greenthread's Complaint

| U.S. Patent No. 11,121,222 | Accused Products |
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| [Claim 1, Element 4] transistors formed in at least one of the first active region or second active region; | The Western Digital Accused Products meet this limitation. <i>See</i> Exhibit A-1, Claim 1, Element 4. |
| [Claim 1, Element 5] at least a portion of at least one of the first and second active regions having at least one graded dopant concentration to aid carrier movement from the first and second active regions towards an area of the substrate where there are no active regions; and | The Western Digital Accused Products meet this limitation. <i>See</i> Exhibit A-1, Claim 1, Element 5. For example, referencing the SRP graph discussed at Exhibit A-1, Claim 1, Element 5, there are no active regions at depths of about 1.3 μm and greater. <i>See also</i> SRP analysis reproduced at Exhibit A-1, Claim 1, Element 5 electrically characterizing the accused product and showing carrier movement and electric fields. SRP analysis generally is discussed at Exhibit A-1, Claim 1, Element 5. |
| [Claim 1, Element 6] at least one well region adjacent to the first or second active region containing at least one graded dopant region, the graded dopant region to aid carrier movement from the surface towards the area of the substrate where there are no active regions, wherein at least some of the transistors form digital logic of the VLSI semiconductor device. | The Western Digital Accused Products meet this limitation. <i>See</i> Exhibit A-2, Claim 1, Element 6. Upon information and belief, at least some of the transistors form digital logic of the VLSI semiconductor device. For example, transistors are commonly used to implement digital logic, e.g., for controlling access to memory components/functionality. Details regarding transistors in the Western Digital Accused Products are in the possession of the Defendants and are expected to be obtained through discovery. <i>See also</i> SRP analysis reproduced at Exhibit A-1, Claim 1, Element 5 electrically characterizing the accused product and showing carrier movement and electric fields. SRP analysis generally is discussed at Exhibit A-1, Claim 1, Element 5. |
| 2. The VLSI semiconductor device of claim 1, wherein the substrate is a p-type substrate. | The Western Digital Accused Products meet this limitation. <i>See</i> Exhibit A-1, Claim 2. |
| 3. The VLSI semiconductor device of claim 1, wherein the substrate has epitaxial silicon on top of a nonepitaxial substrate. | The Western Digital Accused Products meet this limitation. <i>See</i> Exhibit A-1, Claim 4. |
| 4. The VLSI semiconductor device of claim 1, wherein the first active region and second | The Western Digital Accused Products meet this limitation. <i>See</i> Exhibit A-1, Claim 5; Exhibit A-2, Claim 4. Upon information and belief, the first and second active regions contain digital logic as claimed. <i>See</i> above at Claim 1, Element 6. |

Exhibit A-3 to Greenthread's Complaint

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| active region contain digital logic formed by one of either p-channel and n-channel devices. | |
| 5. The VLSI semiconductor device of claim 1, wherein the first active region and second active region contain either p-channel or n-channel devices in n-wells or p-wells, respectively, and each well has at least one graded dopant. | The Western Digital Accused Products meet this limitation. <i>See</i> Exhibit A-1, Claim 6. |
| 6. The VLSI semiconductor device of claim 1, wherein the first active region and second active region are each separated by at least one isolation region. | The Western Digital Accused Products meet this limitation. <i>See</i> Exhibit A-1, Claim 7. |
| 7. The VLSI semiconductor device of claim 1, wherein the graded dopant is fabricated with an ion implantation process. | The Western Digital Accused Products meet this limitation. <i>See</i> Exhibit A-1, Claim 8. |
| 8. The VLSI semiconductor device of claim 1, wherein the first and second active regions are formed adjacent the first surface of the substrate. | The Western Digital Accused Products meet this limitation. <i>See</i> Exhibit A-1, Claim 1, Elements 1-3. |
| 9. The VLSI semiconductor device of claim 1, wherein dopants of the graded dopant concentration in the first active region or the second active region are either p-type or n-type. | The Western Digital Accused Products meet this limitation. <i>See</i> Exhibit A-2, Claim 9. |
| 13. The VLSI semiconductor device of claim 1, wherein the | The Western Digital Accused Products meet this limitation. <i>See</i> Exhibit A-2, Claim 13. Upon information and belief, the transistors which can be formed in the first and second active regions are CMOS digital logic transistors as claimed. <i>See</i> above at Claim 1, Element 6. |

Exhibit A-3 to Greenthread's Complaint

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| transistors which can be formed in the first and second active regions are CMOS digital logic transistors requiring at least a source, a drain, a gate and a channel. | |
| 15. The VLSI semiconductor device of claim 1, wherein the device is a complementary metal oxide semiconductor (CMOS) with a nonepitaxial substrate. | The Western Digital Accused Products meet this limitation. <i>See</i> Exhibit A-2, Claim 15. |
| 16. The VLSI semiconductor device of claim 1, wherein the device is a flash memory. | The Western Digital Accused Products meet this limitation. <i>See</i> Exhibit A-2, Claim 16. |
| 17. The VLSI semiconductor device of claim 1, wherein the device comprises digital logic and capacitors. | The Western Digital Accused Products meet this limitation. Upon information and belief, the semiconductor device comprises digital logic and capacitors. <i>See</i> above at Claim 1, Element 6 (discussion regarding digital logic). Details regarding digital logic and capacitors in the Western Digital Accused Products are in the possession of the Defendants and are expected to be obtained through discovery. |
| 20. The VLSI semiconductor device of claim 1, wherein each of the first and second active regions are in the lateral or vertical direction. | The Western Digital Accused Products meet this limitation. As shown by SEM imaging (<i>see</i> Exhibit A-1, Claim 1, Elements 1-3), each of the first and second active regions are in the lateral or vertical direction. |
| [Claim 21, Preamble] A VLSI semiconductor device, comprising: | To the extent the preamble is a limitation, the Western Digital Accused Products include a semiconductor device. <i>See</i> above at Claim 1, Preamble. |
| [Claim 21, Element 1] a substrate of a first doping type at a first doping level having a surface; | The Western Digital Accused Products meet this limitation. <i>See</i> above at Claim 1, Element 1. |
| [Claim 21, Element 2] a first active region disposed adjacent the surface of the substrate with a second doping type opposite in | The Western Digital Accused Products meet this limitation. <i>See</i> Exhibit A-1, Claim 9, Element 2. |

Exhibit A-3 to Greenthread's Complaint

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| conductivity to the first doping type and within which transistors can be formed in the surface thereof; | |
| [Claim 21, Element 3] a second active region separate from the first active region disposed adjacent to the first active region and within which transistors can be formed in the surface thereof; | The Western Digital Accused Products meet this limitation. <i>See</i> Exhibit A-1, Claim 9, Element 3. |
| [Claim 21, Element 4] transistors formed in at least one of the first active region or second active region; | The Western Digital Accused Products meet this limitation. <i>See</i> Exhibit A-1, Claim 1, Element 4. |
| [Claim 21, Element 5] at least a portion of at least one of the first and second active regions having at least one graded dopant concentration to aid carrier movement from the surface to an area of the substrate where there are no active regions; and | The Western Digital Accused Products meet this limitation. <i>See</i> above at Claim 1, Element 5. <i>See also</i> SRP analysis reproduced at Exhibit A-1, Claim 1, Element 5 electrically characterizing the accused product and showing carrier movement and electric fields. SRP analysis generally is discussed at Exhibit A-1, Claim 1, Element 5. |
| [Claim 21, Element 6] at least one well region adjacent to the first or second active region containing at least one graded dopant region, the graded dopant region to aid carrier movement from the surface to the area of the substrate where there are no active regions, and wherein the graded dopant concentration is linear, quasilinear, error function, complementary error function, or any combination thereof. | The Western Digital Accused Products meet this limitation. <i>See</i> Exhibit A-2, Claim 1, Element 6. As shown by SRP analysis (<i>see</i> Exhibit A-1, Claim 1, Element 1), the graded dopant concentration is linear, quasilinear, error function, complementary error function, or any combination thereof. For example, the quasilinear nature of the concentration is shown in the SRP graph discussed at Exhibit A-1, Claim 1, Element 5. <i>See also</i> SRP analysis reproduced at Exhibit A-1, Claim 1, Element 5 electrically characterizing the accused product and showing carrier movement and electric fields. SRP analysis generally is discussed at Exhibit A-1, Claim 1, Element 5. |

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| 23. The VLSI semiconductor device of claim 21, wherein the substrate is a p-type substrate. | The Western Digital Accused Products meet this limitation. <i>See</i> Exhibit A-1, Claim 2. |
| 24. The VLSI semiconductor device of claim 21, wherein the substrate has epitaxial silicon on top of a nonepitaxial substrate. | The Western Digital Accused Products meet this limitation. <i>See</i> Exhibit A-1, Claim 4. |
| 25. The VLSI semiconductor device of claim 21, wherein the first active region and second active region contain at least one of either p-channel and n-channel devices. | The Western Digital Accused Products meet this limitation. <i>See</i> Exhibit A-1, Claim 5. |
| 26. The VLSI semiconductor device of claim 21, wherein the first active region and second active region contain either p-channel or n-channel devices in n-wells or p-wells, respectively, and each well has at least one graded dopant. | The Western Digital Accused Products meet this limitation. <i>See</i> Exhibit A-1, Claim 6. |
| 27. The VLSI semiconductor device of claim 21, wherein the first active region and second active region are each separated by at least one isolation region. | The Western Digital Accused Products meet this limitation. <i>See</i> Exhibit A-1, Claim 7. |
| 28. The VLSI semiconductor device of claim 21, wherein dopants of the graded dopant concentration in the first active region or the second active region are either p-type or n-type. | The Western Digital Accused Products meet this limitation. <i>See</i> Exhibit A-2, Claim 9. |
| 32. The VLSI semiconductor device of claim 21, wherein the | The Western Digital Accused Products meet this limitation. <i>See</i> Exhibit A-1, Claim 8. |

Exhibit A-3 to Greenthread's Complaint

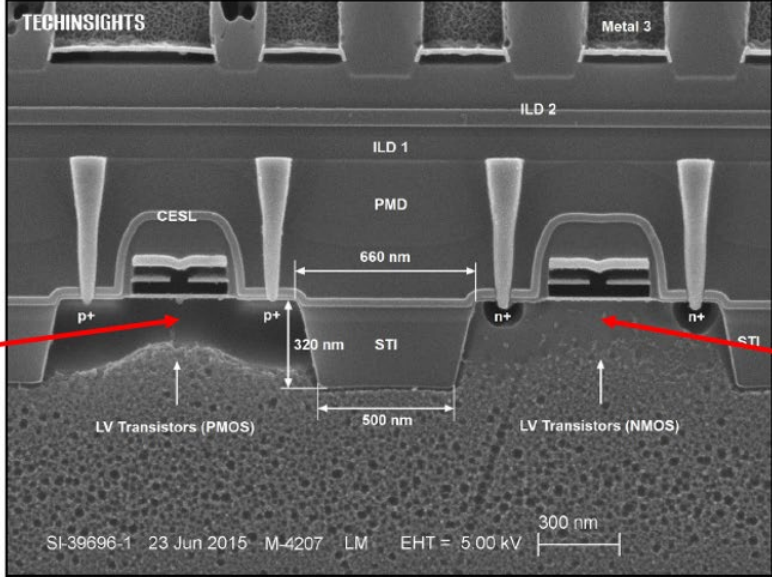
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| graded dopant is fabricated with an ion implantation process. | |
| 33. The VLSI semiconductor device of claim 21, wherein the substrate is a complementary metal oxide semiconductor (CMOS) device. | The Western Digital Accused Products meet this limitation. <i>See</i> Exhibit A-2, Claim 15. |
| 34. The VLSI semiconductor device of claim 21, wherein the device is a flash memory. | The Western Digital Accused Products meet this limitation. <i>See</i> Exhibit A-2, Claim 16. |
| 38. The VLSI semiconductor device of claim 21, wherein each of the first and second active regions are in the lateral or vertical direction. | <p>The Western Digital Accused Products meet this limitation. As shown by SEM imaging (<i>see</i> Figure 2.3.9 shown below and discussed at Exhibit A-1, Claim 1, Element 3), each of the first and second active regions are in the lateral or vertical direction.</p>  <p>Figure 2.3.9: LV logic NMOS and PMOS transistor, SEM cross-sectional image with Si etch</p> |

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| [Claim 39, Preamble] A semiconductor device, comprising: | To the extent the preamble is a limitation, the Western Digital Accused Products include a semiconductor device. <i>See</i> Exhibit A-1, Claim 1, Preamble. |
| [Claim 39, Element 1] a substrate of a first doping type at a first doping level; | The Western Digital Accused Products meet this limitation. <i>See</i> Exhibit A-1, Claim 1, Element 1. |
| [Claim 39, Element 2] a first active region disposed adjacent to a surface of the substrate with a second doping type opposite in conductivity to the first doping type and within which transistors can be formed; | The Western Digital Accused Products meet this limitation. <i>See</i> Exhibit A-1, Claim 1, Element 2. |
| [Claim 39, Element 3] a second active region separate from the first active region disposed adjacent to the first active region and within which transistors can be formed; | The Western Digital Accused Products meet this limitation. <i>See</i> Exhibit A-1, Claim 1, Element 3. |
| [Claim 39, Element 4] transistors formed in at least one of the first active region or second active region; and | The Western Digital Accused Products meet this limitation. <i>See</i> Exhibit A-1, Claim 1, Element 4. |
| [Claim 39, Element 5] at least a portion of at least one of the first and second active regions having at least one graded dopant concentration to aid carrier movement from the first or second active region to at least one substrate area where there is no active region. | The Western Digital Accused Products meet this limitation. <i>See</i> Exhibit A-1, Claim 1, Element 5; <i>see</i> above at Claim 21, Element 5. <i>See also</i> SRP analysis reproduced at Exhibit A-1, Claim 1, Element 5 electrically characterizing the accused product and showing carrier movement and electric fields. SRP analysis generally is discussed at Exhibit A-1, Claim 1, Element 5. |
| 40. The semiconductor device of claim 39 further comprising at least one well region adjacent to | The Western Digital Accused Products meet this limitation. <i>See</i> Exhibit A-2, Claim 1, Element 6. <i>See also</i> SRP analysis reproduced at Exhibit A-1, Claim 1, Element 5 electrically characterizing the accused product and showing carrier movement and electric fields. SRP analysis generally is discussed at Exhibit A-1, Claim 1, Element 5. |

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| the first or second active region and containing at least one graded dopant region, the graded dopant region to aid carrier movement from any region in the well to the substrate area where there is no well. | |
| [Claim 41, Preamble] A semiconductor device, comprising: | To the extent the preamble is a limitation, the Western Digital Accused Products include a semiconductor device. <i>See</i> above at Claim 39, Preamble. |
| [Claim 41, Element 1] a substrate of a first doping type at a first doping level; | The Western Digital Accused Products meet this limitation. <i>See</i> Exhibit A-1, Claim 1, Element 1. |
| [Claim 41, Element 2] a first active region disposed adjacent to a surface of the substrate with a second doping type opposite in conductivity to the first doping type and within which transistors can be formed; | The Western Digital Accused Products meet this limitation. <i>See</i> above at Claim 39, Element 2. |
| [Claim 41, Element 3] a second active region separate from the first active region disposed adjacent to the first active region and within which transistors can be formed; | The Western Digital Accused Products meet this limitation. <i>See</i> above at Claim 39, Element 3. |
| [Claim 41, Element 4] transistors formed in at least one of the first active region or second active region; and | The Western Digital Accused Products meet this limitation. <i>See</i> Exhibit A-1, Claim 1, Element 4. |
| [Claim 41, Element 5] at least a portion of at least one of the first and second active regions having at least one graded dopant acceptor concentration to aid | The Western Digital Accused Products meet this limitation. <i>See</i> above at Claim 21, Element 5. The following graph obtained via SRP analysis reveals at least one graded dopant acceptor concentration (e.g., concentration in p-well) as claimed. |

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| <p>carrier movement from the first or second active region to at least one substrate area where there is no active region.</p> | <div data-bbox="856 207 1650 683"> <p>Figure 2.1.5: Periphery p-well in n-doped Si substrate, spreading resistance profile</p> </div> <p><i>See also</i> SRP analysis reproduced at Exhibit A-1, Claim 1, Element 5 electrically characterizing the accused product and showing carrier movement and electric fields. SRP analysis generally is discussed at Exhibit A-1, Claim 1, Element 5.</p> |
| <p>[Claim 42, Preamble] A semiconductor device, comprising:</p> | <p>To the extent the preamble is a limitation, the Western Digital Accused Products include a semiconductor device. <i>See</i> above at Claim 39, Preamble.</p> |
| <p>[Claim 42, Element 1] a substrate of a first doping type at a first doping level;</p> | <p>The Western Digital Accused Products meet this limitation. <i>See</i> Exhibit A-1, Claim 1, Element 1.</p> |
| <p>[Claim 42, Element 2] a first active region disposed adjacent to a surface of the substrate with a second doping type opposite in conductivity to the first doping type and within which transistors can be formed;</p> | <p>The Western Digital Accused Products meet this limitation. <i>See</i> above at Claim 39, Element 2.</p> |
| <p>[Claim 42, Element 3] a second active region separate from the first active region</p> | <p>The Western Digital Accused Products meet this limitation. <i>See</i> above at Claim 39, Element 3.</p> |

Exhibit A-3 to Greenthread's Complaint

| U.S. Patent No. 11,121,222 | Accused Products |
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| disposed adjacent to the first active region and within which transistors can be formed; | |
| [Claim 42, Element 4] transistors formed in at least one of the first active region or second active region; and | The Western Digital Accused Products meet this limitation. <i>See</i> Exhibit A-1, Claim 1, Element 4. |
| [Claim 42, Element 5] at least a portion of at least one of the first and second active regions having at least one graded donor dopant concentration to aid carrier movement from the first or second active region to at least one substrate area where there is no active region. | The Western Digital Accused Products meet this limitation. SRP analysis (<i>see</i> Exhibit A-1, Claim 1, Element 5) reveals at least one graded dopant acceptor concentration (e.g., concentration in n-well) as claimed. <i>See also</i> SRP analysis reproduced at Exhibit A-1, Claim 1, Element 5 electrically characterizing the accused product and showing carrier movement and electric fields. SRP analysis generally is discussed at Exhibit A-1, Claim 1, Element 5. |
| [Claim 44, Preamble] A CMOS Semiconductor device comprising: | To the extent the preamble is a limitation, the Western Digital Accused Products include a CMOS Semiconductor device. <i>See</i> Exhibit A-1, Claim 1, Preamble; Exhibit A-1, Claim 18. |
| [Claim 44, Element 1]: a surface layer; | The Western Digital Accused Products meet this limitation. <i>See</i> above at Claim 21, Element 1. |

Exhibit A-3 to Greenthread's Complaint

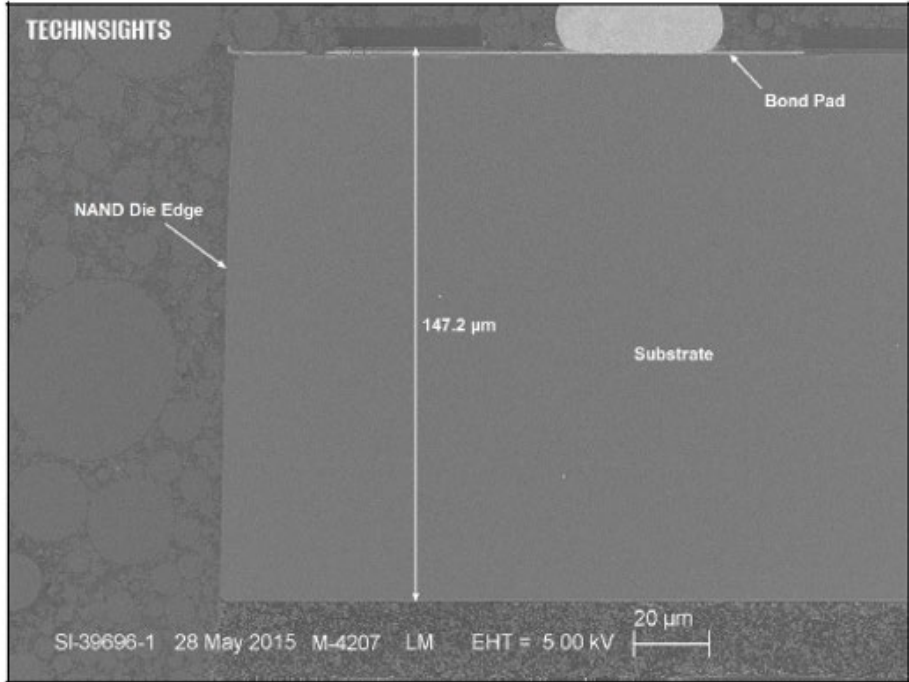
| U.S. Patent No. 11,121,222 | Accused Products |
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| |  <p>TECHINSIGHTS</p> <p>NAND Die Edge</p> <p>147.2 μm</p> <p>Bond Pad</p> <p>Substrate</p> <p>SI-39696-1 28 May 2015 M-4207 LM EHT = 5.00 kV 20 μm</p> <p>← surface layer</p> <p>Figure 1.2.3: Die thickness, SEM cross-sectional image</p> |
| [Claim 44, Element 2] a substrate; | The Western Digital Accused Products meet this limitation. <i>See</i> above at Claim 44, Element 1. |

Exhibit A-3 to Greenthread's Complaint

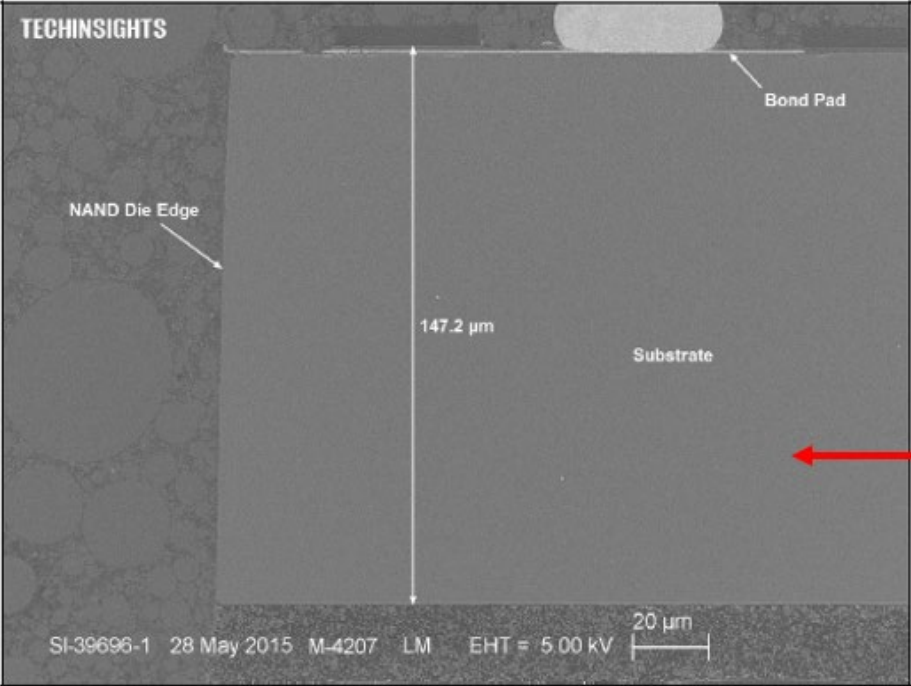
| U.S. Patent No. 11,121,222 | Accused Products |
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| |  <p data-bbox="716 911 1398 943">Figure 1.2.3: Die thickness, SEM cross-sectional image</p> |
| <p data-bbox="111 1000 464 1117">[Claim 44, Element 3] an active region including a source and a drain, disposed on one surface of the surface layer;</p> | <p data-bbox="491 984 1990 1101">The Western Digital Accused Products meet this limitation. <i>See</i> Exhibit A-1, Claim 1, Element 3. For example, the SEM image below (discussed at Exhibit A-1, Claim 1, Element 3) shows that the Sandisk flash memory includes an active region including a source and a drain disposed on one surface of the surface layer (e.g., as shown in the SEM image above for Claim 44, Element 2, the surface layer includes one surface facing away from the substrate (the active region is disposed on this surface) and another surface facing towards the substrate).</p> |

Exhibit A-3 to Greenthread's Complaint

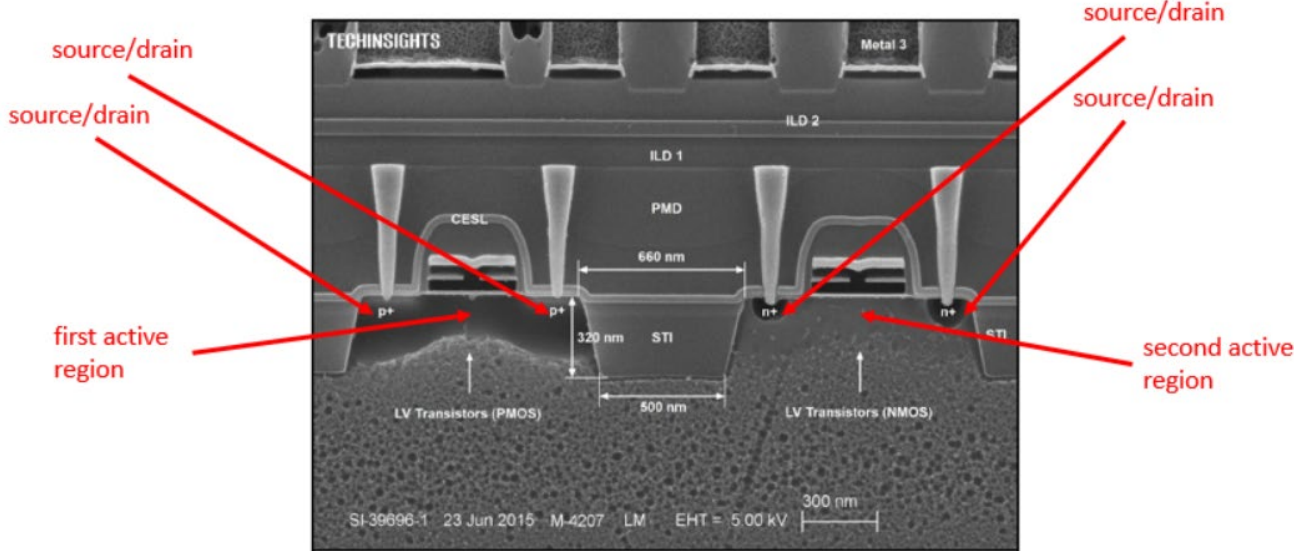
| U.S. Patent No. 11,121,222 | Accused Products |
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| |  <p>Figure 2.3.9: LV logic NMOS and PMOS transistor, SEM cross-sectional image with Si etch</p> |
| <p>[Claim 44, Element 4] a single drift layer disposed between the other surface of the surface layer and the substrate, the drift layer having a graded concentration of dopants extending between the surface layer and the substrate, the drift layer further having a first static unidirectional electric drift field to aid the movement of carriers from the surface layer to an area of the substrate where there are no active regions; and</p> | <p>The Western Digital Accused Products meet this limitation. <i>See</i> above at Claim 21, Element 5. For example, SRP analysis shows that the SanDisk flash memory includes a single drift layer having a graded concentration (annotated with green oval below) as claimed:</p> |

Exhibit A-3 to Greenthread's Complaint

| U.S. Patent No. 11,121,222 | Accused Products |
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| | <div data-bbox="688 203 1816 950" data-label="Figure"> <p>The graph, titled "n-Well Depth Profile", plots Carrier Concentration (cm^{-3}) on a logarithmic y-axis (from $1\text{E}+13$ to $1\text{E}+18$) against Depth (μm) on a linear x-axis (from 0 to 4). Red squares represent the n-well carrier concentration, which starts at approximately $1\text{E}+17.5$ at 0 μm, rises to a peak of $1\text{E}+18$ at 0.7 μm, and then drops sharply to $1\text{E}+14$ by 1.2 μm. Blue diamonds represent the p-substrate carrier concentration, which remains at $1\text{E}+14$ until 1.2 μm, then rises to a plateau of approximately $1\text{E}+14.5$ from 1.5 μm to 4 μm. A green oval highlights the peak of the n-well concentration, and a red bracket above it is labeled "drift layer". The region of the n-well is labeled "n-Well", and the region of the p-substrate is labeled "p-Substrate".</p> </div> <p data-bbox="919 966 1596 1031">Figure 2.1.4: Periphery n-well in p-doped Si substrate, spreading resistance profile</p> <p data-bbox="489 1063 2024 1218">Upon information and belief, the drift layer has a first static unidirectional electric drift field to aid the movement of carriers from the surface layer to an area of the substrate where there are no active regions as claimed, as a result of the above-discussed graded concentration of dopants. Details regarding electric field characteristics are in the possession of the Defendants and are expected to be obtained through discovery. <i>See also</i> SRP analysis reproduced at Exhibit A-1, Claim 1, Element 5 electrically characterizing the accused product and showing carrier movement and electric fields. SRP analysis generally is discussed at Exhibit A-1, Claim 1, Element 5.</p> |

Exhibit A-3 to Greenthread's Complaint

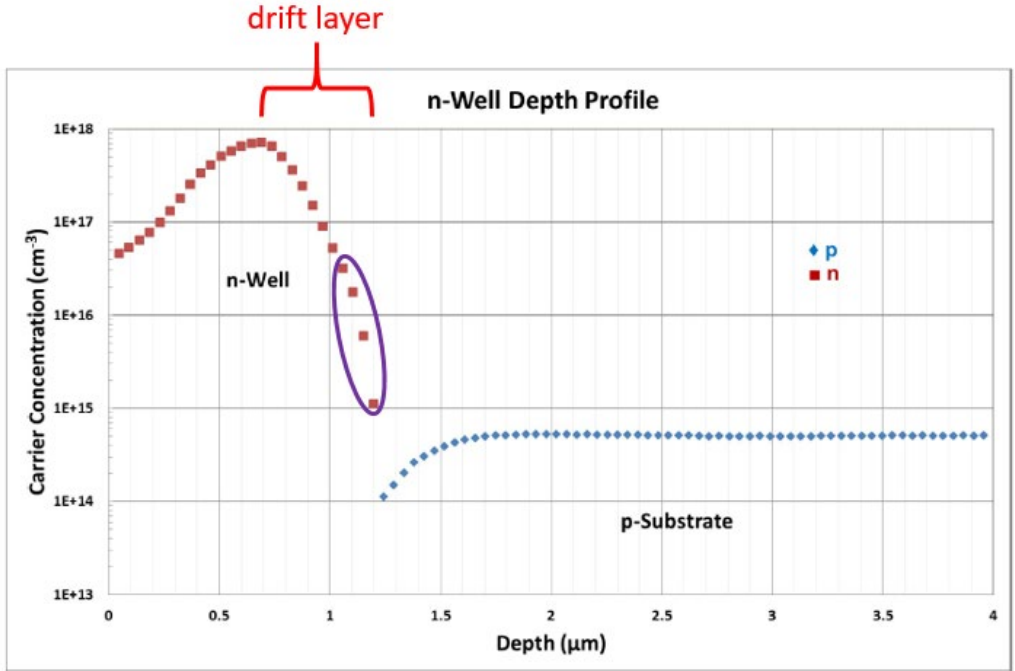
| U.S. Patent No. 11,121,222 | Accused Products |
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| <p>[Claim 44, Element 5] at least one well region disposed in the single drift layer, the well region having a graded concentration of dopants and a second static unidirectional electric drift field to aid the movement of carriers from the surface layer to the area of the substrate where there are no active regions.</p> | <p>The Western Digital Accused Products meet this limitation. <i>See</i> above at Claim 21, Element 6. The well region (discussed above for Claim 21, Element 6) has a graded concentration of dopants (annotated with purple oval below to indicate a region of relatively steeper slope in concentration, compared to the shallower region discussed for Claim 44, Element 4).</p>  <p>Figure 2.1.4: Periphery n-well in p-doped Si substrate, spreading resistance profile</p> <p>Upon information and belief, the well region is disposed in the single drift layer, and it has a second static unidirectional electric drift field to aid the movement of carriers from the surface layer to the area of the substrate where there are no active regions as claimed, as a result of the well region's graded concentration of dopants. Details regarding electric field characteristics are in the possession of the Defendants and are expected to be obtained through discovery. <i>See also</i> SRP analysis reproduced at Exhibit A-1, Claim 1, Element 5 electrically characterizing the accused product and showing carrier movement and electric fields. SRP analysis generally is discussed at Exhibit A-1, Claim 1, Element 5.</p> |

Exhibit A-4 to Greenthread's Complaint

| U.S. Patent No. 8,421,195 | Accused Products |
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| <p>[Claim 1, Preamble] A CMOS Semiconductor device comprising:</p> | <p>To the extent the preamble is a limitation, the Western Digital Accused Products include a CMOS semiconductor device. <i>See</i> Exhibit A-3, Claim 44, Preamble. The SanDisk 15 nm 16 GB NAND flash memory referenced in Exhibit A-1 is discussed in this claim chart and other infringement contention claim charts as an example of a flash memory representative of the Western Digital Accused Products. Upon information and belief, such a SanDisk flash memory is representative of flash memory devices used in the Western Digital Accused Products for purposes of this claim chart and the other infringement contention claim charts because, e.g., other flash memory devices used in Western Digital Accused Products would have similarly been advantageously designed to move carriers (e.g., towards the substrate) and achieve the performance enhancements described and claimed in the '195 patent (and the other asserted patents). For example, other flash memory devices would similarly have been designed with a dopant gradient in order to improve performance characteristics such as on and off switching times and other performance enhancements described in the Abstract of the '195 patent (and the other asserted patents). Therefore, upon information and belief, other flash memory devices used in Western Digital Accused Products contain similar features as the SanDisk 15 nm 16 GB NAND flash memory, and function in a similar way with respect to the features claimed in the asserted claims.</p> <p>This claim chart is based on publicly available information, and additional information regarding these and other accused products is expected to be obtained through discovery.</p> |
| <p>[Claim 1, Element 1] a surface layer;</p> | <p>The Western Digital Accused Products meet this limitation. <i>See</i> Exhibit A-3, Claim 44, Element 1.</p> |
| <p>[Claim 1, Element 2] a substrate;</p> | <p>The Western Digital Accused Products meet this limitation. <i>See</i> Exhibit A-3, Claim 44, Element 2.</p> |
| <p>[Claim 1, Element 3] an active region including a source and a drain, disposed on one surface of said surface layer;</p> | <p>The Western Digital Accused Products meet this limitation. <i>See</i> Exhibit A-3, Claim 44, Element 3.</p> |
| <p>[Claim 1, Element 4] a single drift layer disposed between the other surface of said surface layer and said substrate, said drift layer having a graded concentration of dopants extending between said surface layer and said substrate, said drift layer further having a first static unidirectional electric drift field to aid the movement of minority carriers from said surface layer to said substrate; and</p> | <p>The Western Digital Accused Products meet this limitation. <i>See</i> Exhibit A-3, Claim 44, Element 4. Upon information and belief, the drift layer (<i>see</i> Exhibit A-3, Claim 44, Element 4) has a first static unidirectional electric drift field to aid the movement of minority carriers from the surface layer to the substrate, as claimed. Details regarding electric field characteristics are in the possession of the Defendants and are expected to be obtained through discovery. <i>See also</i> SRP analysis reproduced at Exhibit A-1, Claim 1, Element 5 electrically characterizing the accused product and showing carrier movement and electric fields. SRP analysis generally is discussed at Exhibit A-1, Claim 1, Element 5.</p> |
| <p>[Claim 1, Element 5] at least one well region disposed in said single</p> | <p>The Western Digital Accused Products meet this limitation. <i>See</i> Exhibit A-3, Claim 44, Element 5. Upon information and belief, the well region has a second static unidirectional electric drift field to aid the movement of minority carriers from the surface layer to the substrate, as claimed. Details regarding electric field characteristics are in the possession of the Defendants and are expected to be obtained through</p> |

Exhibit A-4 to Greenthread's Complaint

| U.S. Patent No. 8,421,195 | Accused Products |
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| drift layer, said well region having a graded concentration of dopants and a second static unidirectional electric drift field to aid the movement of minority carriers from said surface layer to said substrate. | discovery. <i>See also</i> SRP analysis reproduced at Exhibit A-1, Claim 1, Element 5 electrically characterizing the accused product and showing carrier movement and electric fields. SRP analysis generally is discussed at Exhibit A-1, Claim 1, Element 5. |
| 2. The CMOS Semiconductor device of claim 1, wherein the said drift layer is a deeply-implanted layer. | The Western Digital Accused Products meet this limitation. Upon information and belief, the drift layer is a deeply-implanted layer. |
| 3. The CMOS Semiconductor device of claim 1, wherein said drift layer is an epitaxial layer. | The Western Digital Accused Products meet this limitation. <i>See</i> Exhibit A-1, Claim 4; Exhibit A-3, Claim 44, Element 4. Upon information and belief, the drift layer is grown above the substrate and is an epitaxial layer. |
| 5. The CMOS Semiconductor device of claim 1, wherein said graded concentration follows a quasi-linear gradient. | The Western Digital Accused Products meet this limitation. <i>See</i> Exhibit A-1, Claim 1, Elements 1, 5. |
| 6. The CMOS Semiconductor device of claim 1, wherein said graded concentration follows an exponential gradient. | The Western Digital Accused Products meet this limitation. <i>See</i> Exhibit A-1, Claim 1, Elements 1, 5. |

Exhibit A-5 to Greenthread's Complaint

| U.S. Patent No. 9,190,502 | Accused Products |
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| <p>[Claim 7, Preamble] A semiconductor device comprising:</p> | <p>To the extent the preamble is a limitation, the Western Digital Accused Products include a semiconductor device. <i>See</i> Exhibit A-4, Claim 1, Preamble. The SanDisk 15 nm 16 GB NAND flash memory referenced in Exhibit A-1 is discussed in this claim chart and other infringement contention claim charts as an example of a flash memory representative of the Western Digital Accused Products. Upon information and belief, such a SanDisk flash memory is representative of flash memory devices used in the Western Digital Accused Products for purposes of this claim chart and the other infringement contention claim charts because, e.g., other flash memory devices used in Western Digital Accused Products would have similarly been advantageously designed to move carriers (e.g., towards the substrate) and achieve the performance enhancements described and claimed in the '502 patent (and the other asserted patents). For example, other flash memory devices would similarly have been designed with a dopant gradient in order to improve performance characteristics such as on and off switching times and other performance enhancements described in the Abstract of the '502 patent (and the other asserted patents). Therefore, upon information and belief, other flash memory devices used in Western Digital Accused Products contain similar features as the SanDisk 15 nm 16 GB NAND flash memory, and function in a similar way with respect to the features claimed in the asserted claims.</p> <p>This claim chart is based on publicly available information, and additional information regarding these and other accused products is expected to be obtained through discovery.</p> |
| <p>[Claim 7, Element 1] a surface layer;</p> | <p>The Western Digital Accused Products meet this limitation. <i>See</i> Exhibit A-4, Claim 1, Element 1.</p> |
| <p>[Claim 7, Element 2] a substrate;</p> | <p>The Western Digital Accused Products meet this limitation. <i>See</i> Exhibit A-4, Claim 1, Element 2.</p> |
| <p>[Claim 7, Element 3] an active region including a source and a drain, disposed on one surface of said surface layer;</p> | <p>The Western Digital Accused Products meet this limitation. <i>See</i> Exhibit A-4, Claim 1, Element 3.</p> |
| <p>[Claim 7, Element 4] a single drift layer disposed between the other surface of said surface layer and said substrate, said drift layer having a graded concentration of dopants generating a first static unidirectional electric drift field to aid the movement of minority carriers from said surface layer to said substrate;</p> | <p>The Western Digital Accused Products meet this limitation. <i>See</i> Exhibit A-4, Claim 1, Element 4. The graded concentration of dopants observed via SRP analysis (<i>see</i> Exhibit A-1, Claim 1, Elements 1, 5) generates a first static unidirectional electric drift field to aid the movement of minority carriers, as claimed. <i>See also</i> SRP analysis reproduced at Exhibit A-1, Claim 1, Element 5 electrically characterizing the accused product and showing carrier movement and electric fields. SRP analysis generally is discussed at Exhibit A-1, Claim 1, Element 5.</p> |
| <p>[Claim 7, Element 5] and at least one well region disposed in said single drift layer, said well region having a graded concentration of</p> | <p>The Western Digital Accused Products meet this limitation. <i>See</i> Exhibit A-4, Claim 1, Element 5. <i>See also</i> SRP analysis reproduced at Exhibit A-1, Claim 1, Element 5 electrically characterizing the accused product and showing carrier movement and electric fields. SRP analysis generally is discussed at Exhibit A-1, Claim 1, Element 5.</p> |

Exhibit A-5 to Greenthread's Complaint

| U.S. Patent No. 9,190,502 | Accused Products |
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| dopants generating a second static unidirectional electric drift field to aid the movement of minority carriers from said surface layer to said substrate. | |
| 8. The semiconductor device of claim 7 wherein said first and second static unidirectional electric fields are adapted to respective grading of dopants to aid movements of carriers in respective active regions. | The Western Digital Accused Products meet this limitation. Upon information and belief, the first and second static unidirectional electric fields are adapted to respective grading of dopants to aid movements of carriers in respective active regions. Details regarding the electric fields and active regions are in the possession of the Defendants and are expected to be obtained through discovery. <i>See also</i> SRP analysis reproduced at Exhibit A-1, Claim 1, Element 5 electrically characterizing the accused product and showing carrier movement and electric fields. SRP analysis generally is discussed at Exhibit A-1, Claim 1, Element 5. |
| 11. The semiconductor device of claim 7 wherein the semiconductor device is a flash memory device. | The Western Digital Accused Products meet this limitation. <i>See</i> Exhibit A-2, Claim 16. |

Exhibit A-6 to Greenthread's Complaint

| U.S. Patent No. 11,316,014 | Accused Products |
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| <p>[Claim 1, Preamble] An electronic system, the system comprising:</p> | <p>To the extent the preamble is a limitation, the Western Digital Accused Products include an electronic system. <i>See</i> Exhibit A-1, Claim 1, Preamble; Exhibit A-4, Claim 1, Preamble. Each Western Digital Accused Product is an electronic system, because a computer is an electronic system.</p> <p>The SanDisk 15 nm 16 GB NAND flash memory referenced in Exhibit A-1 is discussed in this claim chart and other infringement contention claim charts as an example of a flash memory representative of the Western Digital Accused Products. Upon information and belief, such a SanDisk flash memory is representative of flash memory devices used in the Western Digital Accused Products for purposes of this claim chart and the other infringement contention claim charts because, e.g., other flash memory devices used in Western Digital Accused Products would have similarly been advantageously designed to move carriers (e.g., towards the substrate) and achieve the performance enhancements described and claimed in the '014 patent (and the other asserted patents). For example, other flash memory devices would similarly have been designed with a dopant gradient in order to improve performance characteristics such as on and off switching times and other performance enhancements described in the Abstract of the '014 patent (and the other asserted patents). Therefore, upon information and belief, other flash memory devices used in Western Digital Accused Products contain similar features as the SanDisk 15 nm 16 GB NAND flash memory, and function in a similar way with respect to the features claimed in the asserted claims.</p> <p>This claim chart is based on publicly available information, and additional information regarding these and other accused products is expected to be obtained through discovery.</p> |
| <p>[Claim 1, Element 1a] at least one semiconductor device, the at least one semiconductor device including:</p> | <p>The Western Digital Accused Products meet this limitation. <i>See</i> Exhibit A-1, Claim 1, Preamble.</p> |
| <p>[Claim 1, Element 1b] a substrate of a first doping type at a first doping level having a surface;</p> | <p>The Western Digital Accused Products meet this limitation. <i>See</i> Exhibit A-3, Claim 1, Element 1.</p> |
| <p>[Claim 1, Element 1c] a first active region disposed adjacent the surface with a second doping type opposite in conductivity to the first doping type and within which transistors can be formed;</p> | <p>The Western Digital Accused Products meet this limitation. <i>See</i> Exhibit A-3, Claim 1, Element 2; Exhibit A-1, Claim 9, Element 2.</p> |
| <p>[Claim 1, Element 1d] a second active region separate from the first active region disposed adjacent to the first active region and within which transistors can be formed;</p> | <p>The Western Digital Accused Products meet this limitation. <i>See</i> Exhibit A-3, Claim 1, Element 3; Exhibit A-1, Claim 9, Element 3.</p> |
| <p>[Claim 1, Element 1e] transistors formed in at least one of the first active region or second active region;</p> | <p>The Western Digital Accused Products meet this limitation. <i>See</i> Exhibit A-3, Claim 1, Element 4.</p> |

Exhibit A-6 to Greenthread's Complaint

| U.S. Patent No. 11,316,014 | Accused Products |
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| [Claim 1, Element 1f] at least a portion of at least one of the first and second active regions having at least one graded dopant concentration to aid carrier movement from the first and second active regions towards an area of the substrate where there are no active regions; and | The Western Digital Accused Products meet this limitation. <i>See</i> Exhibit A-3, Claim 1, Element 5. <i>See also</i> SRP analysis reproduced at Exhibit A-1, Claim 1, Element 5 electrically characterizing the accused product and showing carrier movement and electric fields. SRP analysis generally is discussed at Exhibit A-1, Claim 1, Element 5. |
| [Claim 1, Element 1g] at least one well region adjacent to the first or second active region containing at least one graded dopant region, the graded dopant region to aid carrier movement from the surface towards the area of the substrate where there are no active regions, wherein at least some of the transistors form digital logic of the semiconductor device. | The Western Digital Accused Products meet this limitation. <i>See</i> Exhibit A-3, Claim 1, Element 6; Exhibit A-3, Claim 21, Element 6. <i>See also</i> SRP analysis reproduced at Exhibit A-1, Claim 1, Element 5 electrically characterizing the accused product and showing carrier movement and electric fields. SRP analysis generally is discussed at Exhibit A-1, Claim 1, Element 5. |
| 2. The system of Claim 1, wherein the substrate of the at least one semiconductor device is a p-type substrate. | The Western Digital Accused Products meet this limitation. <i>See</i> Exhibit A-3, Claim 2. |
| 3. The system of Claim 1, wherein the substrate of the at least one semiconductor device has epitaxial silicon on top of a nonepitaxial substrate. | The Western Digital Accused Products meet this limitation. <i>See</i> Exhibit A-3, Claim 3. |
| 4. The system of Claim 1, wherein the first active region and second active region of the at least one semiconductor device contain digital logic formed by one of either p-channel and n-channel devices. | The Western Digital Accused Products meet this limitation. <i>See</i> Exhibit A-3, Claim 4. |
| 5. The system of Claim 1, wherein the first active region and second active region of the at least one semiconductor device contain either p-channel or n-channel | The Western Digital Accused Products meet this limitation. <i>See</i> Exhibit A-3, Claim 5. |

Exhibit A-6 to Greenthread's Complaint

| U.S. Patent No. 11,316,014 | Accused Products |
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| devices in n-wells or p-wells, respectively, and each well has at least one graded dopant. | |
| 6. The system of Claim 1, wherein the first active region and second active region of the at least one semiconductor device are each separated by at least one isolation region. | The Western Digital Accused Products meet this limitation. <i>See</i> Exhibit A-3, Claim 6. |
| 7. The system of Claim 1, wherein the graded dopant is fabricated with an ion implantation process. | The Western Digital Accused Products meet this limitation. <i>See</i> Exhibit A-3, Claim 7. |
| 8. The system of Claim 1, wherein the first and second active regions of the at least one semiconductor device are formed adjacent the first surface of the substrate of the at least one semiconductor device. | The Western Digital Accused Products meet this limitation. <i>See</i> Exhibit A-3, Claim 8. |
| 9. The system of Claim 1, wherein dopants of the graded dopant concentration in the first active region or the second active region of the at least one semiconductor device are either p-type or n-type. | The Western Digital Accused Products meet this limitation. <i>See</i> Exhibit A-3, Claim 9. |
| 13. The system of claim 1, wherein the transistors which can be formed in the first and second active regions of the at least one semiconductor device are CMOS digital logic transistors requiring at least a source, a drain, a gate and a channel. | The Western Digital Accused Products meet this limitation. <i>See</i> Exhibit A-3, Claim 13. |
| 15. The system of Claim 1, wherein the at least one semiconductor device is a complementary metal oxide semiconductor (CMOS) with a nonepitaxial substrate. | The Western Digital Accused Products meet this limitation. <i>See</i> Exhibit A-3, Claim 15. |
| 16. The system of Claim 1, wherein the at least one semiconductor device is a flash memory. | The Western Digital Accused Products meet this limitation. <i>See</i> Exhibit A-3, Claim 16. |

Exhibit A-6 to Greenthread's Complaint

| U.S. Patent No. 11,316,014 | Accused Products |
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| 17. The system of Claim 1, wherein the at least one semiconductor device comprises digital logic and capacitors. | The Western Digital Accused Products meet this limitation. <i>See</i> Exhibit A-3, Claim 17. |
| 20. The system of Claim 1, wherein each of the first and second active regions of the at least one semiconductor device are in the lateral or vertical direction. | The Western Digital Accused Products meet this limitation. <i>See</i> Exhibit A-3, Claim 20. |
| [Claim 21, Preamble] An electronic system, the system comprising: | To the extent the preamble is a limitation, the Western Digital Accused Products include an electronic system. <i>See</i> above at Claim 1, Preamble. |
| [Claim 21, Element 1a] at least one semiconductor device, the at least one semiconductor device including: | The Western Digital Accused Products meet this limitation. <i>See</i> above at Claim 1, Element 1a. |
| [Claim 21, Element 1b] a substrate of a first doping type at a first doping level having a surface; | The Western Digital Accused Products meet this limitation. <i>See</i> above at Claim 1, Element 1b. |
| [Claim 21, Element 1c] a first active region disposed adjacent the surface of the substrate with a second doping type opposite in conductivity to the first doping type and within which transistors can be formed in the surface thereof; | The Western Digital Accused Products meet this limitation. <i>See</i> above at Claim 1, Element 1c; Exhibit A-1, Claim 9, Element 2. |
| [Claim 21, Element 1d] a second active region separate from the first active region disposed adjacent to the first active region and within which transistors can be formed in the surface thereof; | The Western Digital Accused Products meet this limitation. <i>See</i> above at Claim 1, Element 1d; Exhibit A-1, Claim 9, Element 3. |
| [Claim 21, Element 1e] transistors formed in at least one of the first active region or second active region; | The Western Digital Accused Products meet this limitation. <i>See</i> above at Claim 1, Element 1e. |
| [Claim 21, Element 1f] at least a portion of at least one of the first and second active regions having at least one graded dopant concentration to aid carrier movement from the surface to an | The Western Digital Accused Products meet this limitation. <i>See</i> above at Claim 1, Element 1f; Exhibit A-1, Claim 9, Element 5. <i>See also</i> SRP analysis reproduced at Exhibit A-1, Claim 1, Element 5 electrically characterizing the accused product and showing carrier movement and electric fields. SRP analysis generally is discussed at Exhibit A-1, Claim 1, Element 5. |

Exhibit A-6 to Greenthread's Complaint

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| area of the substrate where there are no active regions; and | |
| [Claim 21, Element 1g] at least one well region adjacent to the first or second active region containing at least one graded dopant region, the graded dopant region to aid carrier thereof movement from the surface to the area of the substrate where there are no active regions, and wherein the graded dopant concentration is linear, quasilinear, error function, complementary error function, or any combination thereof. | The Western Digital Accused Products meet this limitation. <i>See</i> above at Claim 1, Element 1g; Exhibit A-3, Claim 21, Element 6. <i>See also</i> SRP analysis reproduced at Exhibit A-1, Claim 1, Element 5 electrically characterizing the accused product and showing carrier movement and electric fields. SRP analysis generally is discussed at Exhibit A-1, Claim 1, Element 5. |
| 23. The system of Claim 21, wherein the substrate of the at least one semiconductor device is a p-type substrate. | The Western Digital Accused Products meet this limitation. <i>See</i> Exhibit A-3, Claim 23. |
| 24. The system of Claim 21, wherein the substrate of the at least one semiconductor device has epitaxial silicon on top of a nonepitaxial substrate. | The Western Digital Accused Products meet this limitation. <i>See</i> Exhibit A-3, Claim 24. |
| 25. The system of Claim 21, wherein the first active region and second active region of the at least one semiconductor device contain at least one of either p-channel and n-channel devices. | The Western Digital Accused Products meet this limitation. <i>See</i> Exhibit A-3, Claim 25. |
| 26. The system of Claim 21, wherein the first active region and second active region of the at least one semiconductor device contain either p-channel or n-channel devices in n-wells or p-wells, respectively, and each well has at least one graded dopant. | The Western Digital Accused Products meet this limitation. <i>See</i> Exhibit A-3, Claim 26. |
| 27. The system of Claim 21, wherein the first active region and second active region of the at least | The Western Digital Accused Products meet this limitation. <i>See</i> Exhibit A-3, Claim 27. |

Exhibit A-6 to Greenthread's Complaint

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| one semiconductor device are each separated by at least one isolation region. | |
| 28. The system of Claim 21, wherein dopants of the graded dopant concentration in the first active region or the second active region of the at least one semiconductor device are either p-type or n-type. | The Western Digital Accused Products meet this limitation. <i>See</i> Exhibit A-3, Claim 28. |